DS35X2GAXXX

3.3V/1.8V x1/x2/x4 2G-bit SPI NAND FLASH

Figure Content

Table Content

Documents title

2Gbit NAND FLASH

Revision History

Revision No.	History	Draft date	Release date	Remark
0.0	Initial Draft	Aug 29, 2018	Aug 31, 2018	preliminary
0.1	Modify random access parameter, bad blocks maximum and change 3.0V to 3.3V	Nov 15, 2018	Nov 18, 2018	
0.2	Modify catalog page number and make title consistent with PN in the content	Jul 5, 2019	Jul 9, 2019	
0.3	Add BGA 24(6x4 ball array) ball definition and package size etc	Sep 3, 2019	Sep 6, 2019	
0.4	Update 1.8V max frequency to 104Mhz	Feb 20，2020	Feb 23，2020	
0.5	Add BGA 24(5x5 ball array) ball definition and package size etc	April 27, 2021	April 30, 2021	
0.6	Modify random data program sequence	Jun 07, 2021	Jun 11, 2021	
0.7	Update drawing sheet of BGA 24(5x5 ball array)	Jul 30, 2021	Aug 03, 2021	
0.8	Modify test condition description of table 4.3	Feb 22，2022	Feb 25，2022	
0.9	Add 105℃Industrial Plus P/N support	Sep 13, 2022	Sep 15, 2022	

FEATURES

■ Serial Peripheral Interface
- Mode 0 and Mode 3

■ Standard, Dual, Quad SPI
- Standard SPI: SCLK, CS#, SI, SO
- Dual SPI: SCLK, CS#, SIO0, SIO1
- Quad SPI: SCLK, CS#, SIO0, SIO1, SIO2, SIO3

■ SUPPLY VOLTAGE
- VCC = 1.8/3.3 Volt core supply voltage for Program, Erase and Read operations

■ PAGE READ / PROGRAM
- (2048+64 spare) byte
- Random access: 25us (w/o ECC), 90us(w/ ECC)
- Serial access: 104MHz (1.8V/3.3V)
- Page program time: 300us (Typ)

■ FAST BLOCK ERASE
- Block size: (128K + 4K) bytes
- Block erase time: 2ms (Typ)

■ MEMORY CELL ARRAY
- (2K + 64) bytes x 64 pages x 2048 blocks

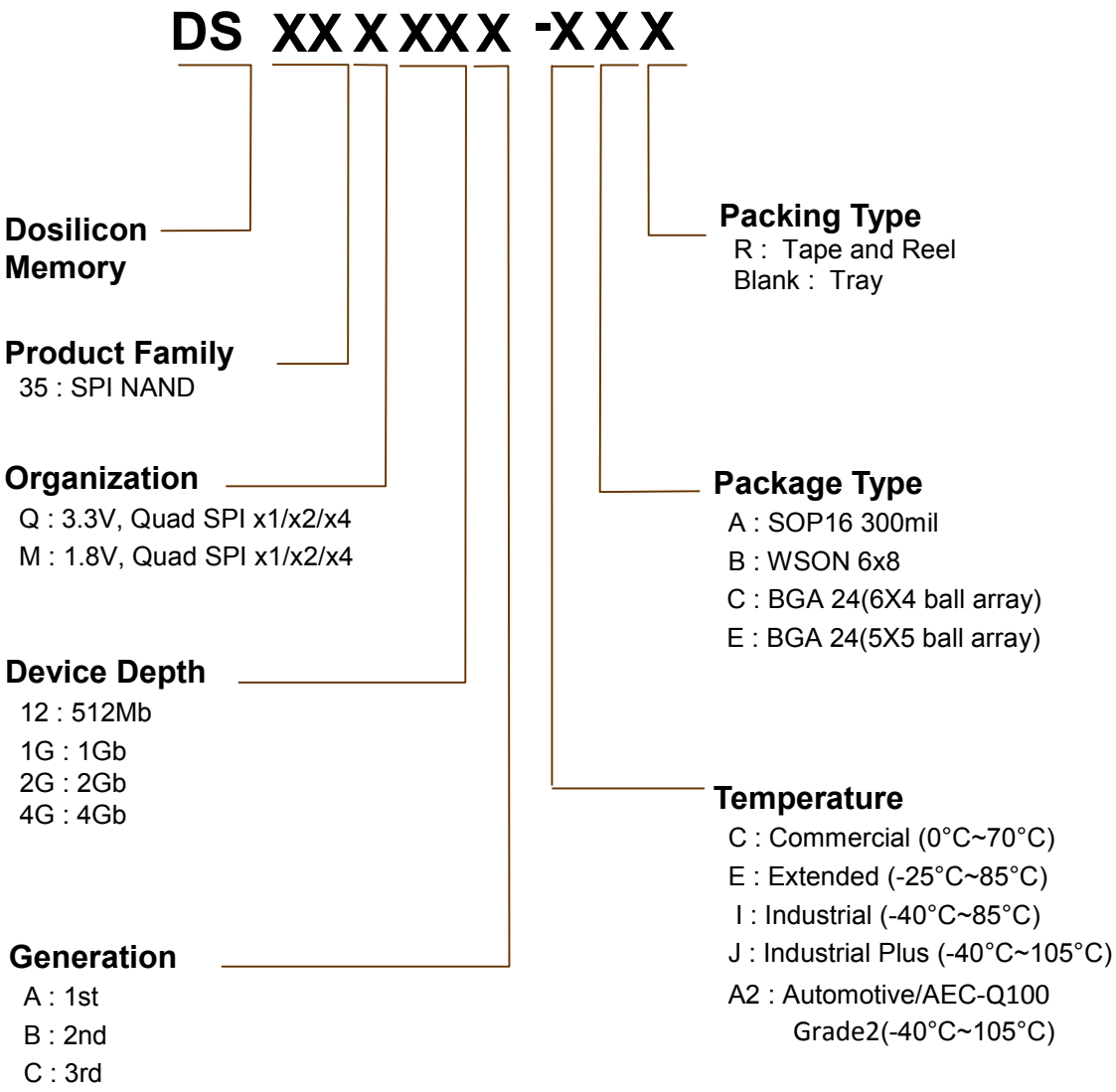
■ ELECTRONIC SIGNATURE
- Manufacturer Code
- Device Code

■ STATUS REGISTER

■ HARDWARE DATA PROTECTION
- Enable/Disable protection with WP# Pin
- Top or Bottom, Block selection combination

■ DATA RETENTION
- Max cycling: 100K Program / Erase cycles
- Data retention: 10 Years (4bit/512byte ECC)
- Internal ECC can be enabled (4bit ECC)
- Block zero is a valid block and will be valid for at least 1K program-erase cycles with ECC

Part Numbering System



1 SUMMARY DESCRIPTION

DS35X2GAXXX is a **256Mx8bit** with spare **8Mx8** bit capacity.
The device is offered in 3.3/1.8 Vcc Power Supply, and with SPI interface.
The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.
The device contains **2048 blocks**, composed by 64 pages consisting in two NAND structures of 32 series connected Flash cells. Program operation allows the 2112-byte page writing in typical 300us and an erase operation can be performed in typical 2 ms on a 128K-byte block.
Data in the page can be read out at **10ns** cycle time per word. The on-chip Program/Erase Controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data.

An internal 4-bit ECC logic is implemented in the chip, which is enabled by default. The internal ECC can be disabled or enabled again by command. When the internal 4-bit ECC logic is disabled, the host side needs to handle the 4-bit ECC by host micro controller.

The serial peripheral interface (SPI) provides NAND Flash with a cost-effective non-volatile memory storage solution in systems where pin count must be kept to a minimum. It is also an alternative to SPI-NOR, offering superior write performance and cost per bit over SPI-NOR.

1.1 Product List

PART NUMBER	ORGANIZATION	VCC RANGE	PACKAGE
DS35M2GA	X1/X2/X4	1.7 – 1.95 Volt	16SOP, 8WSON, BGA24
DS35Q2GA	X1/X2/X4	2.7 – 3.6 Volt	16SOP, 8WSON, BGA24

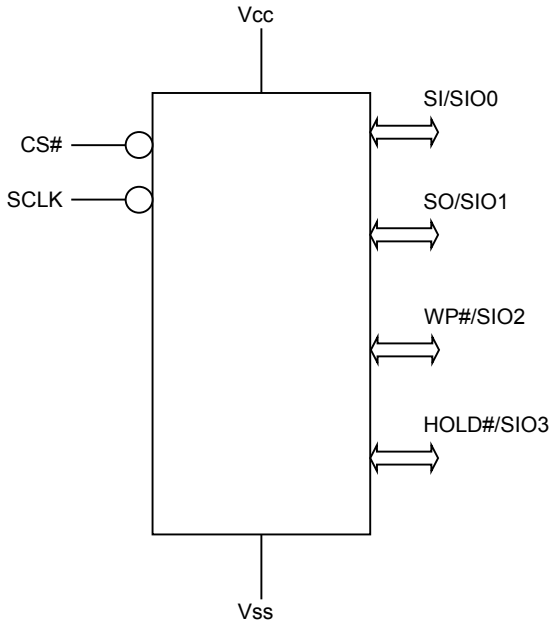


Figure 1.1 Logic Diagram

Name	Function
CS#	Chip Select
SCLK	Clock Input
SI/SIO0	Serial Data Input (for 1 x I/O) or Serial Data Input & Output (for 2xI/O or 4xI/O mode)
SO/SIO1	Serial Data Output (for 1 x I/O) or Serial Data Input & Output (for 2xI/O or 4xI/O mode)
WP#/SIO2	WP# or Serial Data Input & Output (for 4xI/O mode)
HOLD#/SIO3	Hold# or Serial Data Input & Output (for 4xI/O mode)
Vcc	Power supply
Vss	Ground
NC	No Connection

Table 1.1 Signal Name

1.2 Pin description

Pin Name	Description
CS#	**Chip select** Places the device in active power mode when driven LOW. Deselects the device and places SO at High-Z when HIGH
SCLK	**Serial clock** Provides serial interface timing. Latches commands, addresses, and data on SI on the rising edge of SCLK. Triggers output on SO after the falling edge of SCLK.
SI/SIO0	**Serial data input** Transfers data serially into the device. Device latches commands, addresses, and program data on SI on the rising edge of SCLK. SI must not be driven by the host during x2 or x4 read operations.
SO/SIO1	**Serial data output** Transfers data serially out of the device on the falling edge of SCLK.
WP#/SIO2	**Write protect** When LOW, prevents overwriting block-lock bits if the block register write disable (BRWD) bit is set. WP# must not be driven by the host during x4 read operations.
HOLD#/SIO3	**Hold** Pauses any serial communication with the device without deselecting it. When driven LOW, SO is at High-Z, and all inputs at SI and SCLK are ignored. Requires that CS# also be driven LOW. HOLD# must not be driven by the host during x4 read operations.
V_{CC}	**Supply Voltage** The VCC supplies the power for all the operations (Read, Write, Erase).
V_{SS}	**Ground**
NC / DNU	**No Connection / Don't Use**

Table 1.2 Pin Description

1.3 Functional block diagram

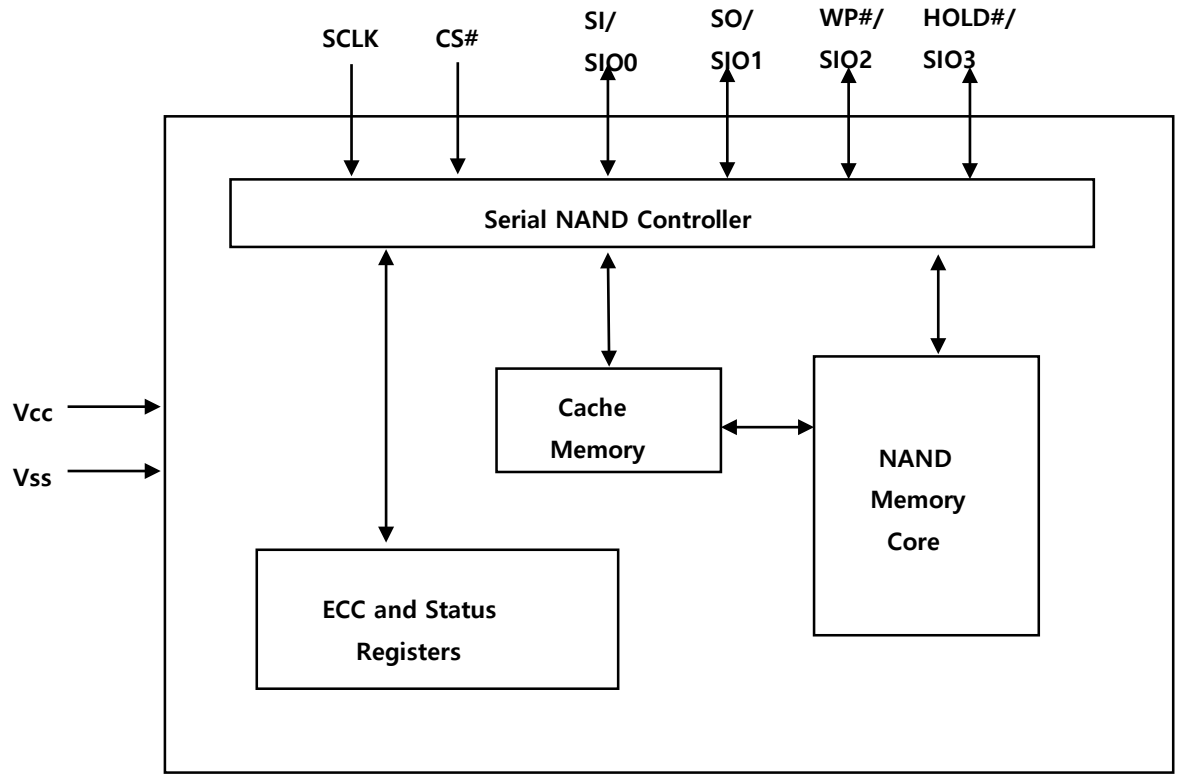


Figure 1.2 Block Description

1.4 Address Map

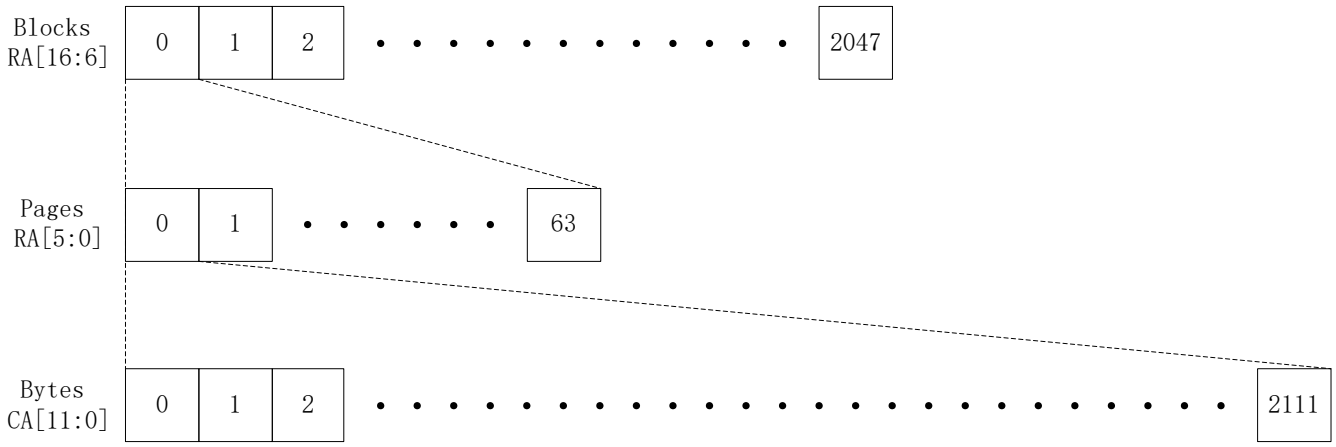


Figure 1.3 Address Map

1.5 Command Set

FUNCTION	Command Code	Address Bytes	Dummy Bytes	Data Bytes	Comments
GET FEATURE	0Fh	1	0	1	Get features
SET FEATURE	1Fh	1	0	1	Set features
WRITE ENABLE	06h	0	0	0	
WRITE DISABLE	04h	0	0	0	
PAGE READ	13h	3	0	0	Array read
READ FROM CACHE	03h, 0Bh	2	1	1 to 2112	Output cache data on SO
READ FROM CACHE x2	3Bh	2	1	1 to 2112	Output cache data on SI and SO
READ FROM CACHE x4	6Bh	2	1	1 to 2112	Output cache data on SI, SO, WP#,HOLD#
PROGRAM LOAD	02h	2	0	1 to 2112	Load program data with cache reset
PROGRAM LOAD x4	32h	2	0	1 to 2112	Load program data on SI, SO, WP#,HOLD# with cache reset
PROGRAM LOAD RANDOM DATA	84h	2	0	1 to 2112	Load program data without cache reset
PROGRAM LOAD RANDOM DATA x4	34h	2	0	1 to 2112	Load program data on SI, SO, WP#,HOLD# without cache reset
PROGRAM EXECUTE	10h	3	0	0	Enter block/page address, no data, execute
BLOCK ERASE	D8h	3	0	0	Block erase
READ ID	9Fh	0	1	2	Read device ID
RESET	FFh	0	0	0	Reset the device

Table 1.3 Command Set

2 BUS OPERATION

2.1 SPI Mode.

Two SPI modes are supported.
• CPOL = 0, CPHA = 0 (Mode 0)
• CPOL = 1, CPHA = 1 (Mode 3)
Input data is latched in on the rising edge of SCLK, and output data is available from the falling edge of SCLK for both modes.
When the bus master is in standby mode:
• SCLK remains at 0 for (CPOL = 0, CPHA = 0 Mode 0)
• SCLK remains at 1 for (CPOL = 1, CPHA = 1 Mode 3)
See **Figure 2.1**

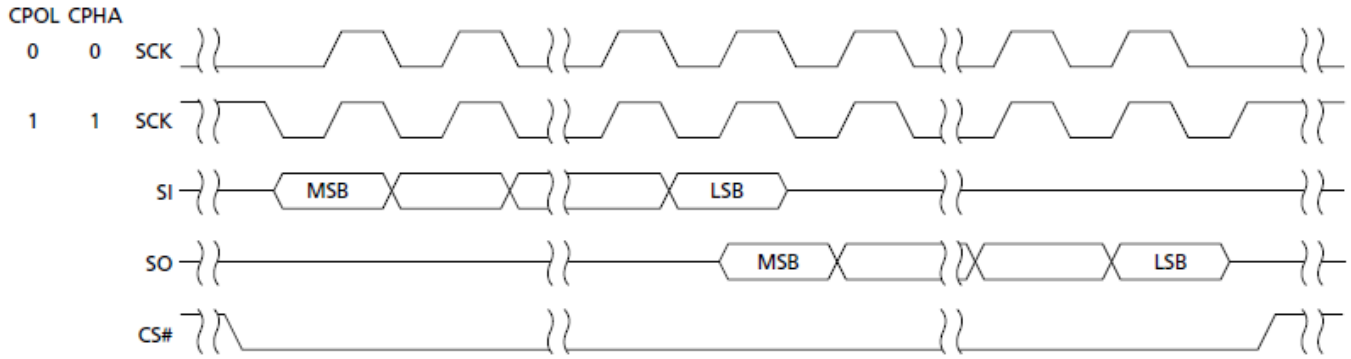


Figure 2.1 SPI Modes Timing

2.2 CS#

Chip select (CS#) activates or deactivates the device. When CS goes LOW, the device is placed in active mode. When CS is HIGH, the device is placed in inactive mode and SO is High-Z.

2.3 SI/SIO0

Writes use serial data in (SI). Data, commands, and addresses are transferred on SI in x1 mode at the rising edge of SCLK. SI must not be driven by the host during x2 or x4 read operations.
SIO0 operation is enabled by issuing a READ FROM CACHE x2 or x4 command with data being clocked out of the device at the falling edge of SCLK. During this time the host must wait until the READ FROM CACHE x2 or x4 command is complete before driving SI.

2.4 SO/SIO1

Reads use serial data out (SO). Device reads are performed in x1, or x2, or x4 modes. SO acts as the only output in x1 READ operations, and as SIO1 in x2 and x4 read operations.
Data is clocked out of the device on SO at the falling edge of SCLK control signals.

2.5 WP#/SIO2

Write protect (WP#) prevents the block lock bits (BP0, BP1, and BP2) from being overwritten.

If the BRWD bit is set to 1 and WP# is LOW, the block protect bits cannot be altered. WP# must not be driven by the host during READ FROM CACHE x4 operations.
SIO2 operation is enabled by issuing a READ FROM CACHE x4 command with data being clocked out of the device at the falling edge of SCLK. During this time the host must wait until the READ FROM CACHE x4 command is complete before driving WP#.

2.6 HOLD#/SIO3

HOLD# input provides a method to pause serial communication with the device but does not terminate any ERASE, READ, or WRITE operation currently in progress.
Hold mode starts at the falling edge of HOLD# provided SCLK is also LOW. If SCLK is HIGH when HOLD# goes LOW, hold mode begins after the next falling edge of SCLK. Similarly, hold mode is exited at the rising edge of HOLD# provided SCLK is also LOW. If SCLK is HIGH, hold mode ends after the next falling edge of SCLK.
During hold mode, SO is High-Z, and SI and SCLK inputs are ignored.
SIO3 operation is enabled by issuing a READ FROM CACHE x4 command with data being clocked out of the device at the falling edge of SCLK. During this time the host must wait until the READ FROM CACHE x4 command is complete before driving HOLD#.

3 DEVICE OPERATION

3.1 Write Operations.

The WRITE ENABLE (06h) command sets the WEL bit in the status register to 1. WRITE ENABLE is required in the following operations that change the contents of the memory array:

- Page program
- OTP program
- BLOCK ERASE

See **Figure 3.1**

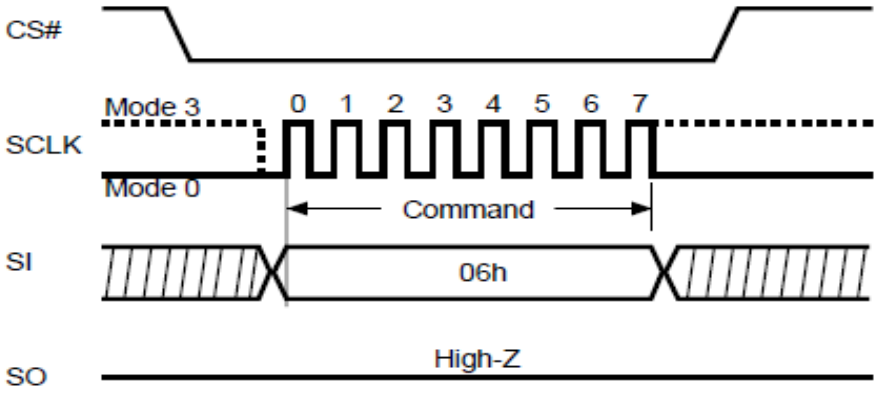


Figure 3.1 Write Enable

The WRITE DISABLE (04h) command clears the WEL bit in the status register to 0. This disables the following operations:

- Page program
- OTP program
- BLOCK ERASE

See **Figure 3.2**

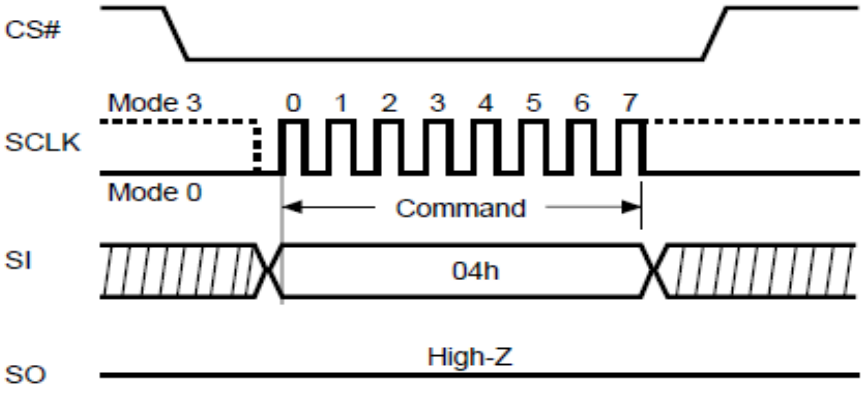


Figure 3.2 Write Disable

3.2 Feature Operations

The GET FEATURES (0Fh) and SET FEATURES (1Fh) commands are used to alter the device behavior from the default power-on behavior. These commands use a 1-byte feature address to determine which feature is to be

read or modified. Features such as OTP and block locking can be enabled or disabled by setting specific bits in feature address A0h and B0h (shown in the following table). The status register is mostly read, except WEL, which is a writable bit with the WRITE ENABLE (06h) command.
When a feature is set, it remains active until the device is power cycled or the feature is written to. Unless specified in the following table, once the device is set, it remains set, even if a RESET (FFh) command is issued. See **Figure 3.3, 3.4.**

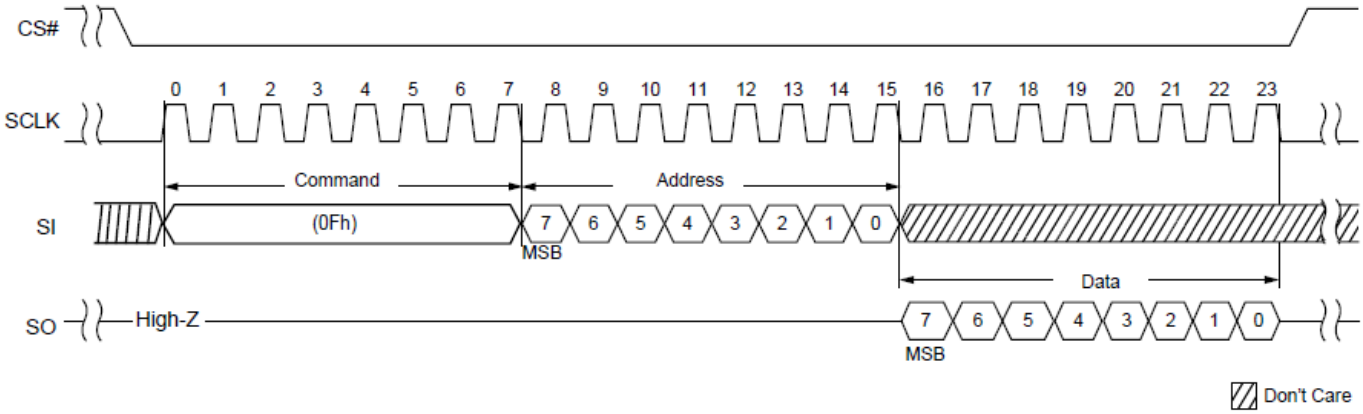


Figure 3.3 Get Features(0Fh)

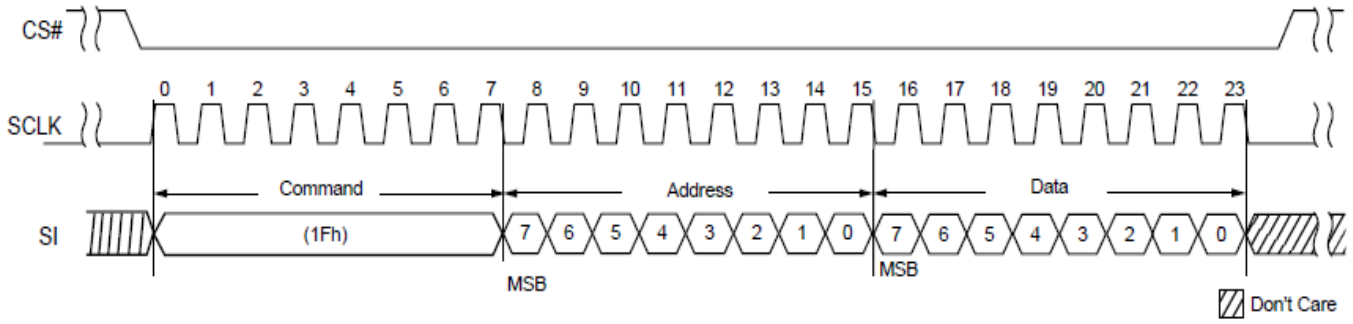


Figure 3.4 Set Features(1Fh)

Register	Address	Data Bits							
		7	6	5	4	3	2	1	0
Block lock	A0h	BRWD	Reserved	BP2	BP1	BP0	INV	CMP	Reserved
OTP	B0h	OTP_PRT	OTP_EN	Reserved	ECC Enable	Reserved	Reserved	Reserved	QE
Status	C0h	Reserved	Reserved	ECC_S1	ECC_S0	P_Fail	E_Fail	WEL	OIP
Driver Strength	D0h	Reserved	DS_IO1	DS_IO0	Reserved	Reserved	Reserved	Reserved	Reserved

Table 3.1 Status Register Coding

3.3 Read Operations.

The device supports "Power-on Read" function, after power up, the device will automatically load the data of the 1st page of 1st block from array to cache. The host micro-controller may directly read the 1st page of 1st block data from the cache buffer. The data is also under the internal ECC protection.

The PAGE READ (13h) command transfers the data from the NAND Flash array to the cache register. The command sequence is follows:

- 13h (PAGE READ to cache)
- 0Fh (GET FEATURES command to read the status)
- 0Bh / 03h / 3Bh / 6Bh (Random data read)

The PAGE READ command requires a 24-bit address consisting of 7 dummy bits followed by a 17-bit block/page address. After the block/page addresses are registered, the device starts the transfer from the main array to the cache register, and is busy for tR time. During this time, the GET FEATURE (0Fh) command can be issued to monitor the status of the operation. Following a status of successful completion, the RANDOM DATA READ (03h or 0Bh) command must be issued in order to read the data out of the cache. The RANDOM DATA READ command requires 3 dummy bits, followed by a 1-bit plane select address and a 12-bit column address for the starting byte address. The starting byte address can be 0 to 2111. The Quad Enable bit (QE) of feature (B0[0]) must be set to enable the read from cache x4 command

See **Figure 3.5, 3.6, 3.7, 3.8**.

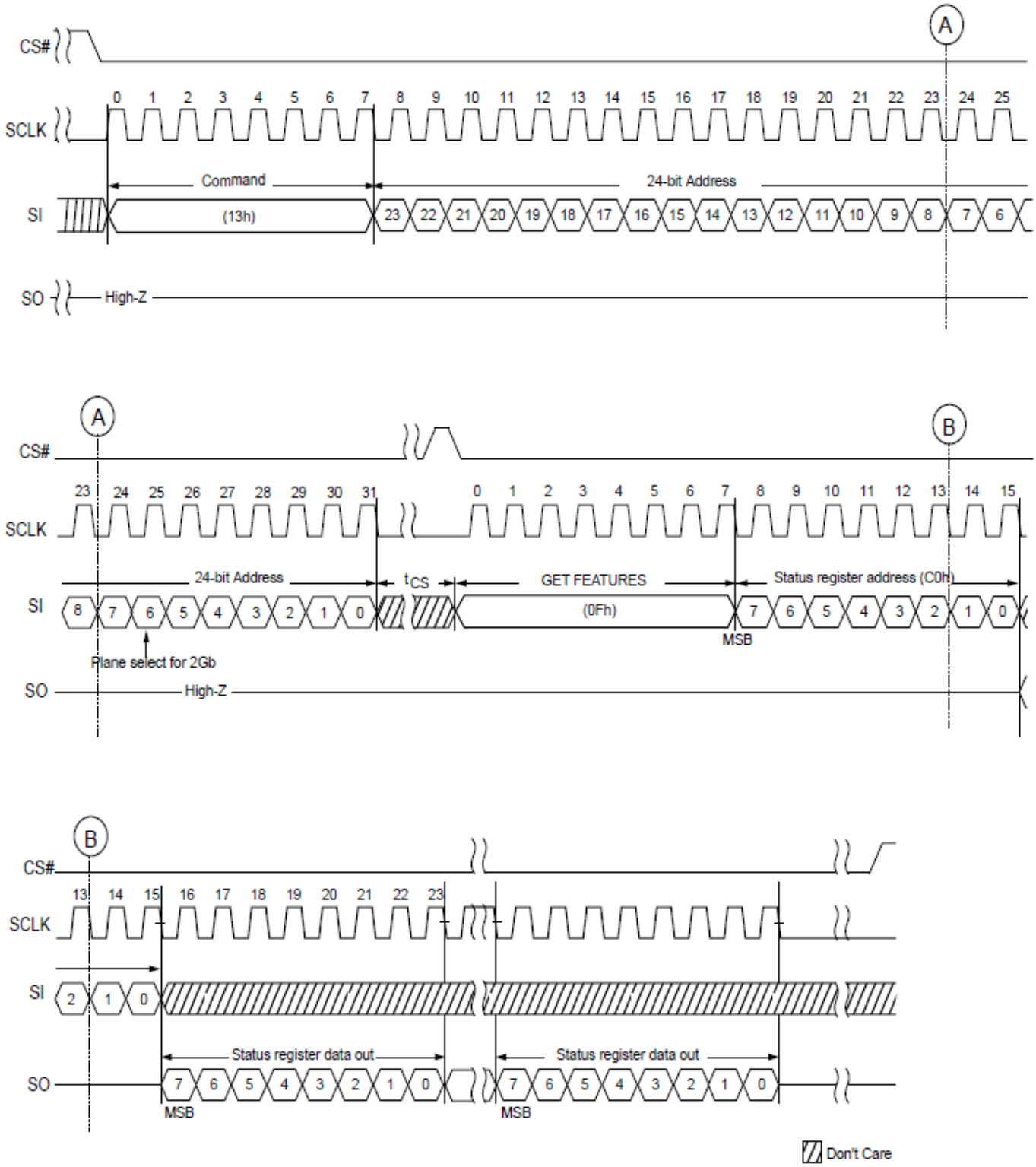


Figure 3.5 Page Read (13h)

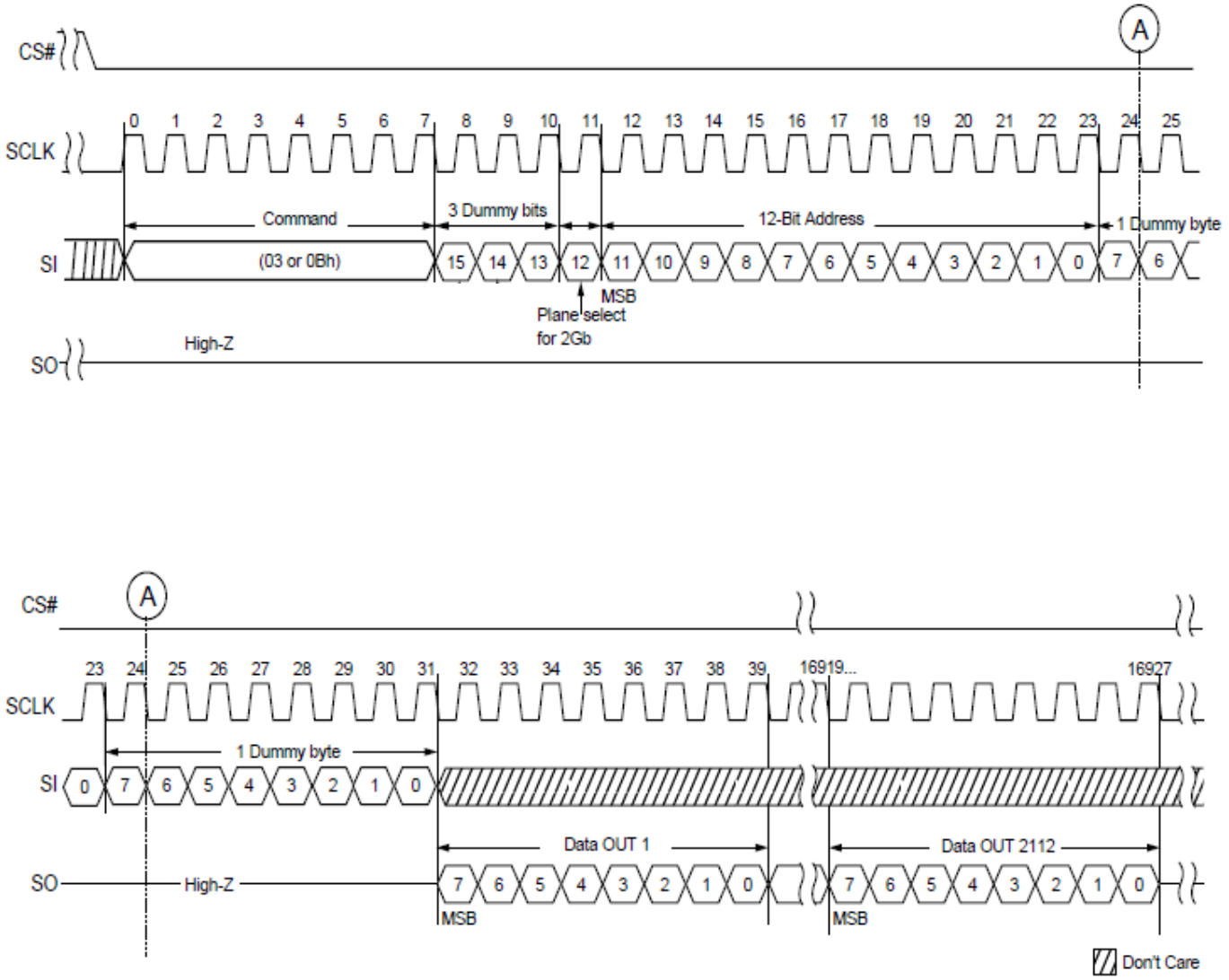


Figure 3.6 Random Data Read (03h or 0Bh)

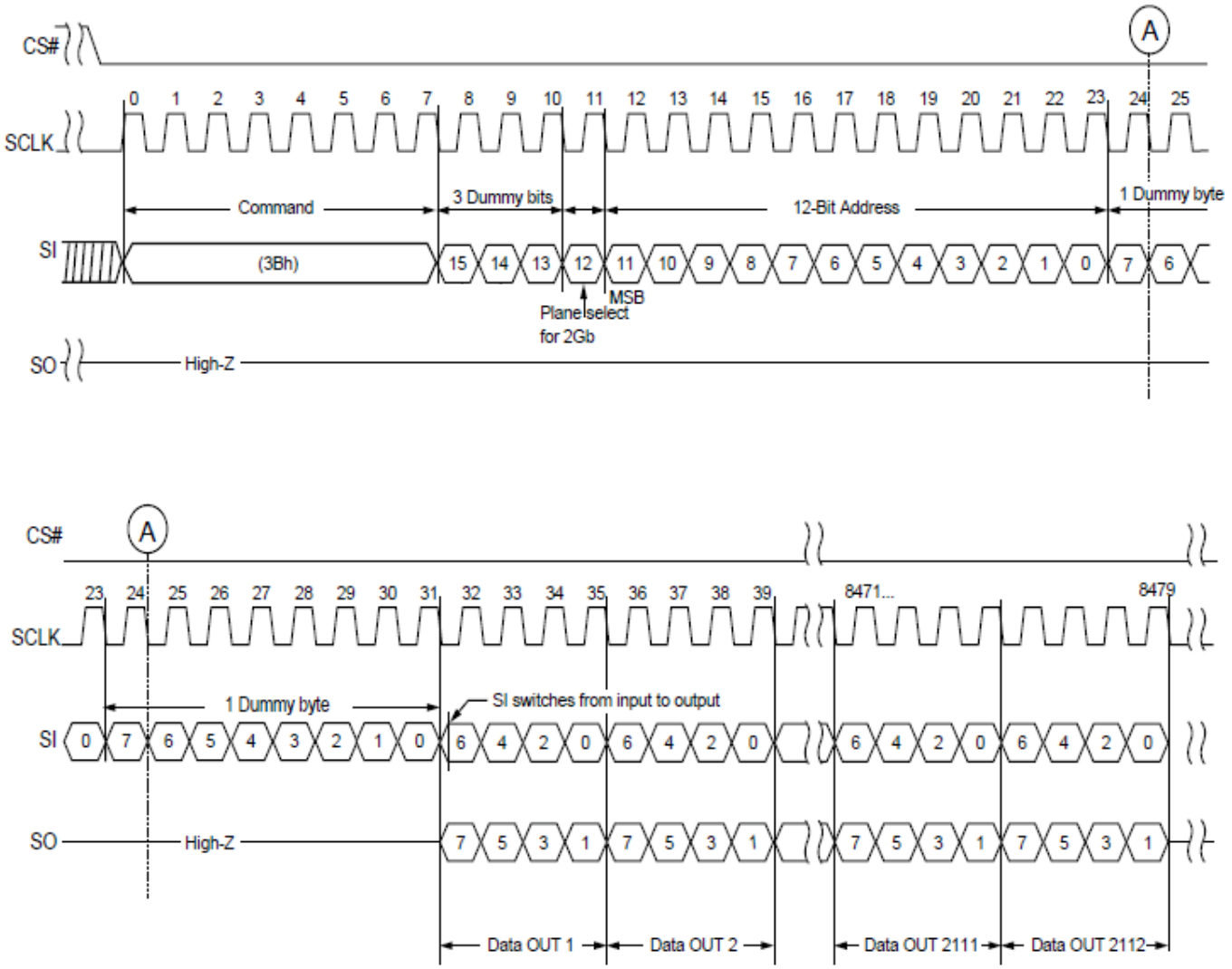


Figure 3.7 Read From Cache x2

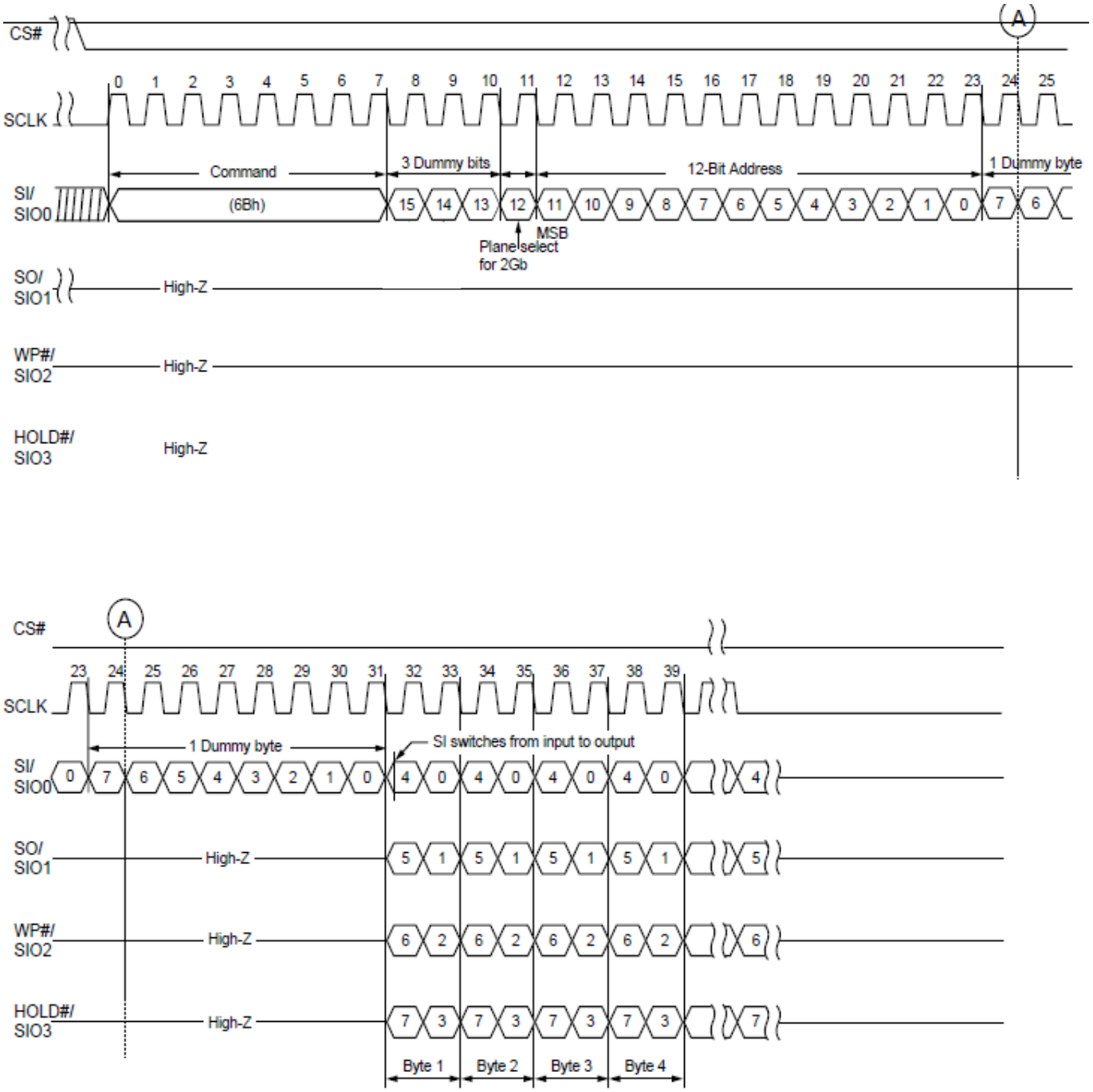


Figure 3.8 Read From Cache x4

The Quad Enable bit (QE) of feature (B0[0]) must be set to enable the read from cache x4 command

3.4 Read ID.

The READ ID command is used to read the 2 bytes of identifier code programmed into the NAND Flash device. The READ ID command reads a 2-byte table (see below) that includes the Manufacturer ID and the device configuration.
See **Figure 3.9**.

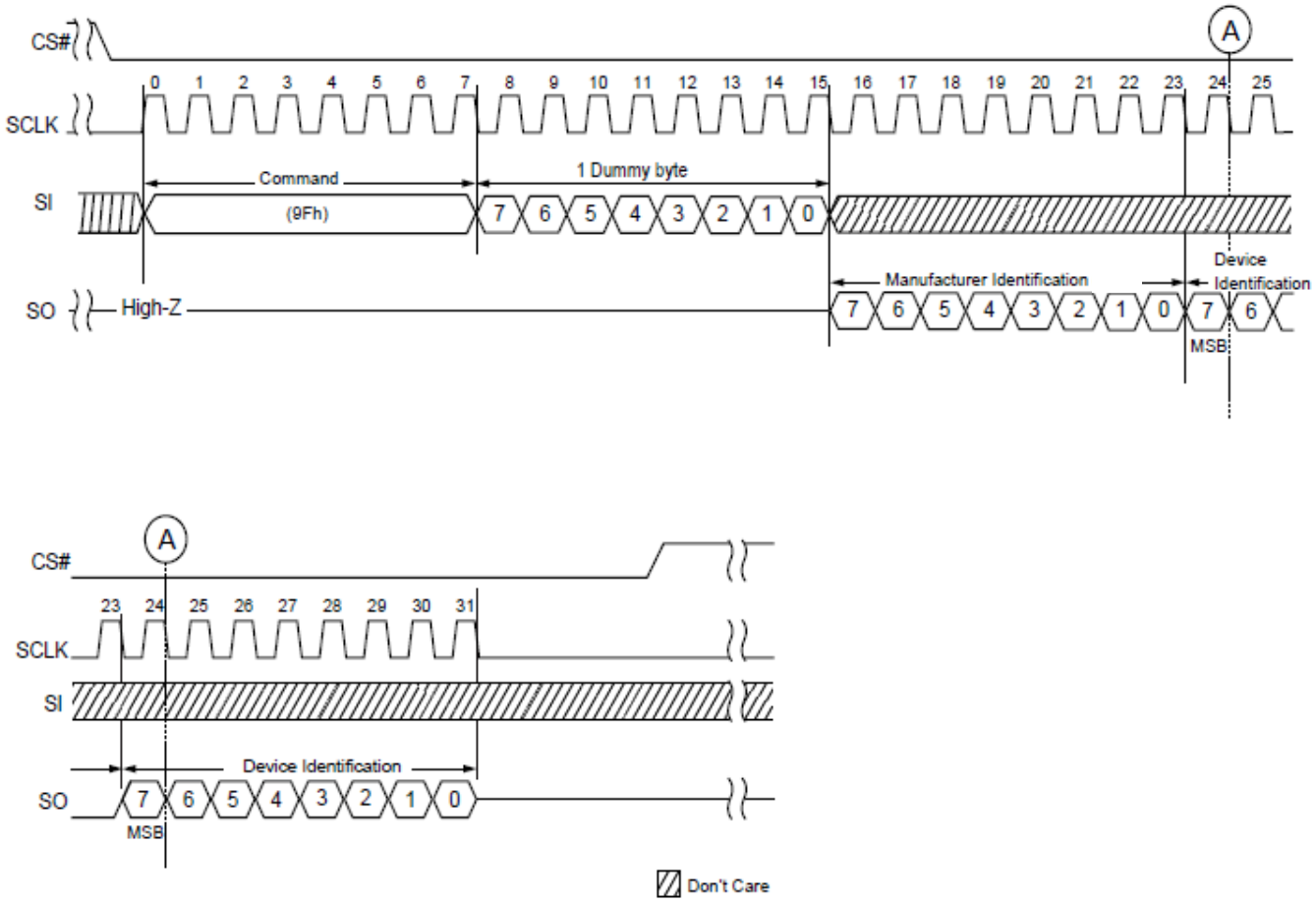


Figure 3.9 Read ID (9Fh)

DENSITY	VCC	1st	2nd
2Gbit	3.3V	E5h	72h
	1.8V	E5h	22h

Table 3.2 Read ID for Supported Configurations

3.5 Parameter Page.

The following command flow must be issued by the memory controller to access the parameter page
1. Issue a SET FEATURES (1Fh) command with a feature address of B0h and data value of 40h (OTP enable, ECC disable).
2. Issue a PAGE READ (13h) command with a block/page address of 0x01h, and then check the status of the read completion using the GET FEATURES (0Fh) command with a feature address of C0h.
3. Issue a READ FROM CACHE (03h) command with an address of 0x00h to read the data out of the NAND device (see the following Parameter Page Data Structure table for a description of the contents of the parameter page.)
4. To exit reading the parameter page, issue a SET FEATURES (1Fh) command with a feature address of B0h and data value of 10h (main array READ, ECC enable).

Byte	Description	Value
0-3	Parameter page signature	4Fh, 4Eh, 46h, 49h
4-5	Revision number	00h, 00h
6-7	Features supported	00h, 00h
8-9	Optional commands supported	06h, 00h
10-31	Reserved (0)	All 00h
32-43	Device manufacturer (12 ASCII characters)	44h, 4Fh, 53h, 49h, 4Ch, 49h, 43h, 4Fh, 4Eh, 20h, 20h, 20h
44-63	Device model (20 ASCII characters)	3.3V: 44h, 53h, 33h, 35h, 51h, 32h, 47h, 41h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h 1.8V: 44h, 53h, 33h, 35h, 4Dh, 32h, 47h, 41h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	JEDEC manufacturer ID	E5h
65-66	Date code	00h, 00h
67-79	Reserved (0)	All 00h
80-83	Number of data bytes per page	00h, 08h, 00h, 00h
84-85	Number of spare bytes per page	40h, 00h
86-89	Number of data bytes per partial page	00h, 02h, 00h, 00h
90-91	Number of spare bytes per partial page	10h, 00h
92-95	Number of pages per block	40h, 00h, 00h, 00h
96-99	Number of blocks per logical unit (LUN)	00h, 08h, 00h, 00h
100	Number of logical units (LUNs)	01h
101	Number of address cycles (N/A)	00h
102	Number of bits per cell	01h
103-104	Bad blocks maximum per LUN	28h, 00h
105-106	Block endurance	01h, 05h
107	Guaranteed valid blocks at beginning of target	01h
108-109	Block endurance for guaranteed valid blocks	01h, 03h
110	Number of programs per page	04h
111	Partial programming attributes	00h
112	Number of bits ECC correctability	00h
113	Number of interleaved address bits	00h
114	Interleaved operation attributes	00h
115-127	Reserved (0)	All 00h
128	I/O pin capacitance	0Ah
129-130	Timing mode support	00h, 00h
131-132	Program cache timing mode support	00h, 00h

Byte	Description	Value
133-134	t_{PROG} Maximum page program time (µs)	BCh, 02h
135-136	t_{BERS} Maximum block erase time (µs)	10h, 27h
137-138	t_R Maximum page read time (µs)	3.3V: 5Ah, 00h 1.8V: 64h, 00h
139-163	Reserved (0)	All 00h
164-165	Vendor specific Revision number	00h, 00h
166-253	Vendor specific	All 00h
254-255	Integrity CRC	3.3V: ADh, B8h 1.8V: 0Bh, 66h
256-511	Value of bytes 0-255	
512-767	Value of bytes 0-255	
768+	Additional redundant parameter pages	FFh

Table 3.3 Parameter Page Data

3.6 UniqueID Page.

The following command flow must be issued by the memory controller to access the uniqueID.
1. Issue a SET FEATURES (1Fh) command with a feature address of B0h and data value of 40h (OTP enable, ECC disable).
2. Issue a PAGE READ (13h) command with a block/page address of 0x00h, and then check the status of the read completion using the GET FEATURES (0Fh) command with a feature address of C0h.
3. Issue a READ FROM CACHE (03h) command with an address of 0x00h to read the data out of the NAND device. (The contents of the uniqueID page are described in the following note.)
Note: The device stores 16 copies of the unique ID data. Each copy is 32 bytes; the first 16 bytes are unique data, and the second 16 bytes are the complement of the first 16 bytes. The host should XOR the first 16 bytes with the second 16 bytes. If the result is 16 bytes of FFh, then that copy of the unique ID data is correct. If a non-FFh result is returned, the host can repeat the XOR operation on a subsequent copy of the unique ID data.
4. To exit reading the uniqueID page, issue a SET FEATURES (1Fh) command with a feature address of B0h and data value of 10h (main array READ, ECC enable).

3.7 Program Operations.

The PAGE PROGRAM operation sequence programs 1 byte to 2112 bytes of data within a page. The page program sequence is as follows:

- 06h (WRITE ENABLE)
- 02h (PROGRAM LOAD) or 32h (PROGRAM LOAD x4)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

Prior to performing the PROGRAM LOAD operation, a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE must be executed in order to set the WEL bit. If this command is not issued, then the rest of the program sequence is ignored. WRITE ENABLE must be followed by a PROGRAM LOAD (02h or 32h) command. PROGRAM LOAD consists of an 8-bit Op code, followed by 3 dummy bits, a 1-bit plane select address and a 12-bit column address, then the data bytes to be programmed. The data bytes are loaded into a cache register that is 2112 bytes long. Only four partial-page programs are allowed on a single page. If more than 2112 bytes are loaded, then those additional bytes are ignored by the cache register. The command sequence ends when CS goes from LOW to HIGH. **Figure 3.10, 3.11** shows the PROGRAM LOAD operation.
After the data is loaded, a PROGRAM EXECUTE (10h) command must be issued to initiate the transfer of data from the cache register to the main array. PROGRAM EXECUTE consists of an 8-bit Op code, followed by a 24-bit

address (7 dummy bits and a 17-bit block/page address). After the page/block address is registered, the memory device starts the transfer from the cache register to the main array, and is busy for tPROG time.
This operation is shown in **Figure 3.12**. During this busy time, the status register can be polled to monitor the status of the operation (refer to the Status Register section). When the operation completes successfully, the next series of data can be loaded with the PROGRAM LOAD command.
See **Figure 3.10, 3.11, 3.12**

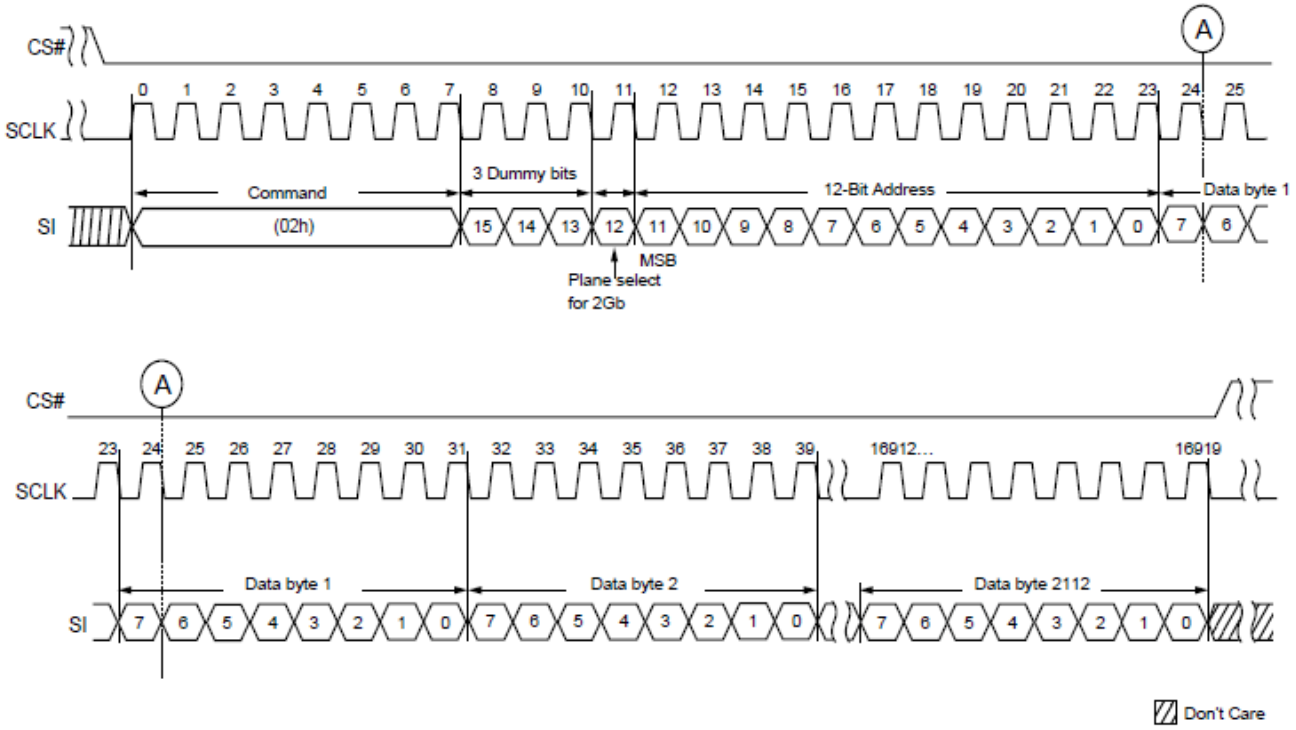


Figure 3.10 Program Load (02h)

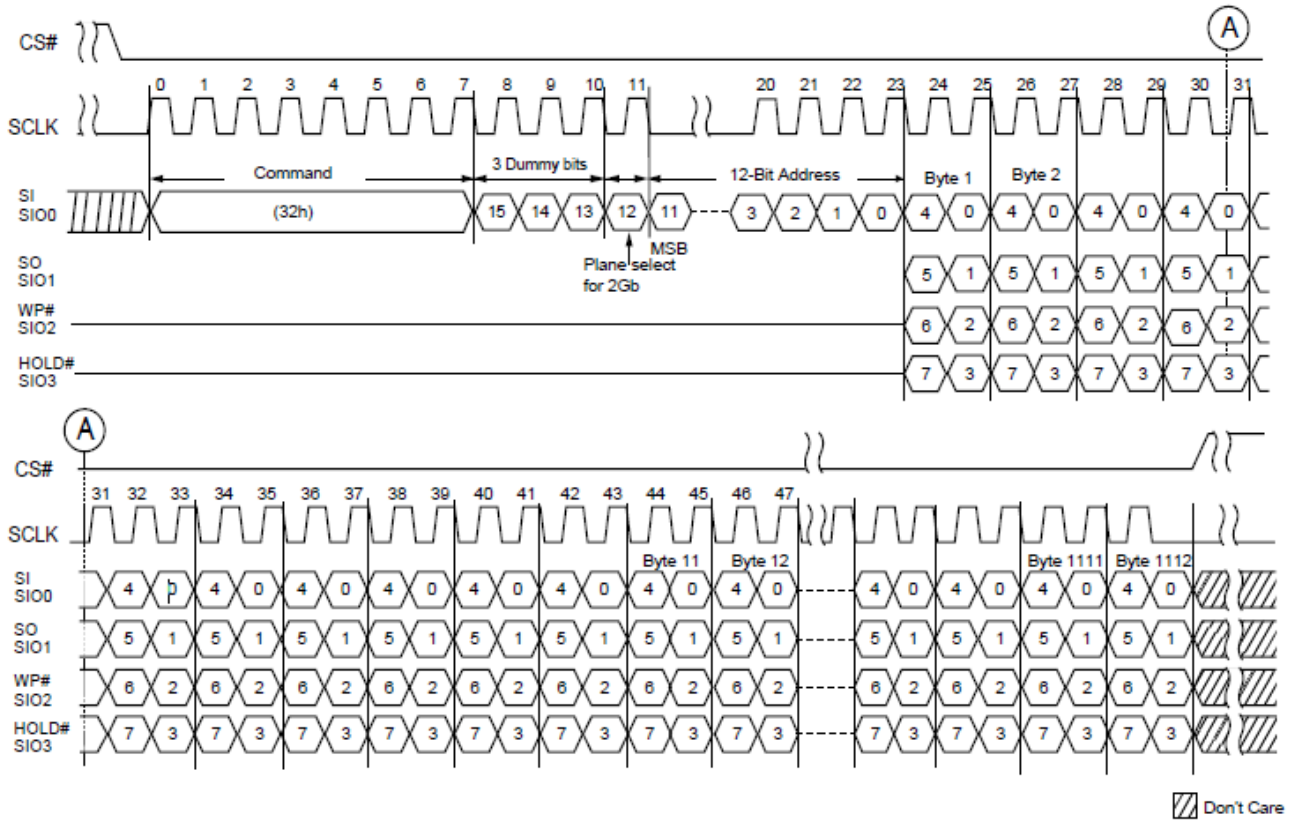


Figure 3.11 Program Load x4 (32h)

The Quad Enable bit (QE) of feature (B0[0]) must be set to enable the program load x4 command.

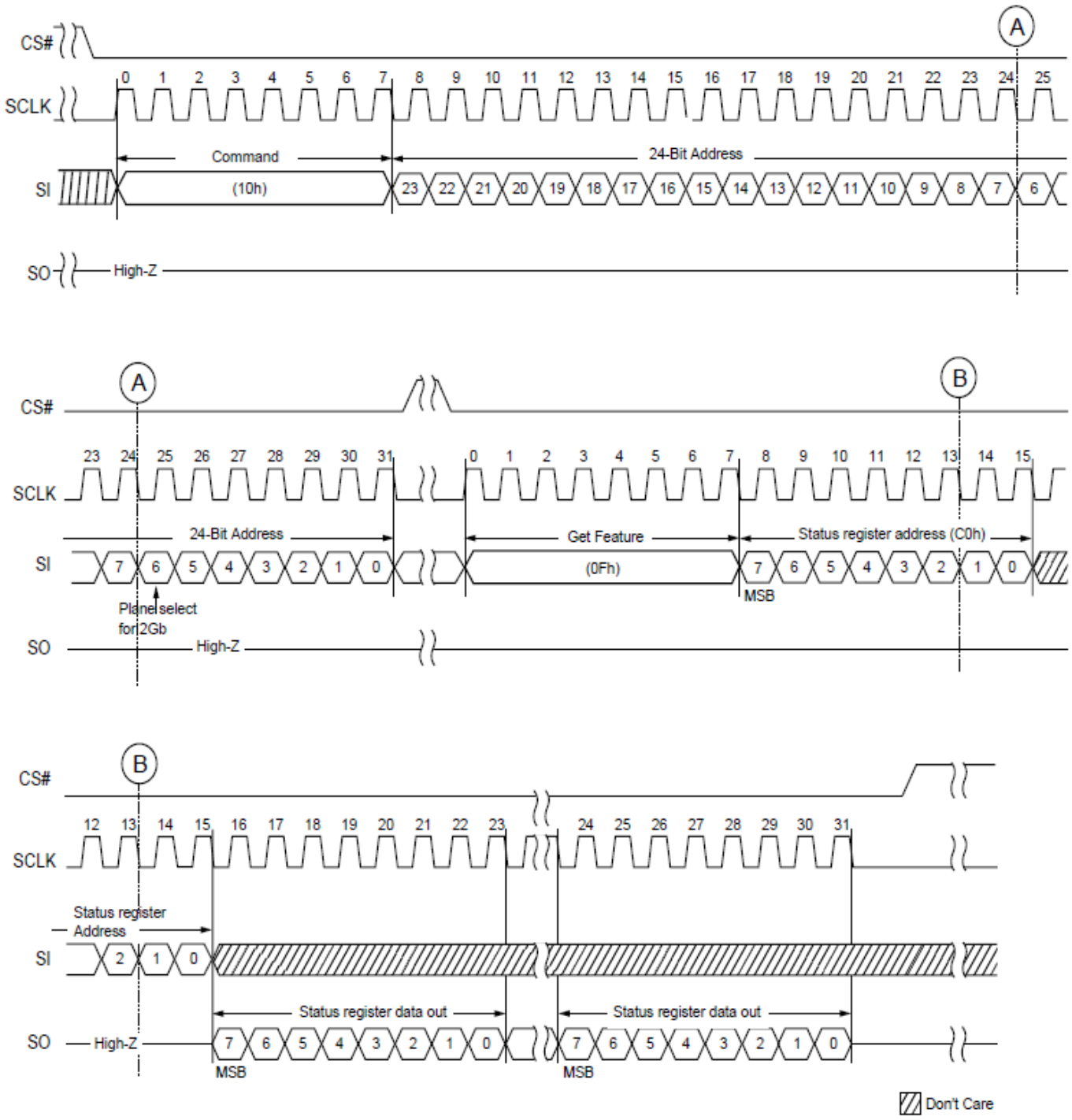


Figure 3.12 Program Excute (10h)

The RANDOM DATA PROGRAM sequence programs or replaces data in a page with existing data. The random data program sequence is as follows:

- 06h (WRITE ENABLE)
- 02h (PROGRAM LOAD) or 32h (PROGRAM LOAD x4)
- 84h (PROGRAM LOAD RANDOM DATA) or 34h (PROGRAM LOAD RANDOM DATA x4)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

Prior to performing a PROGRAM LOAD RANDOM DATA operation, a WRITE ENABLE (06h) command must be issued to change the contents of the memory array. Following a WRITE ENABLE (06) command, first a PROGRAM LOAD (02h or 32h) command must be issued to reset the cache, then issue a PROGRAM LOAD RANDOM DATA (84h or 34h) command. This command consists of an 8-bit Op code, followed by 3 dummy bits, a 1-bit plane select address and a 12-bit column address. New data is loaded in the column address provided with the 12 bits. If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA (84h or 34h) command must be issued with a new column address. After the data is loaded, a PROGRAM EXECUTE (10h) command can be issued to start the programming operation.

See **Figure 3.13, 3.14, 3.12**

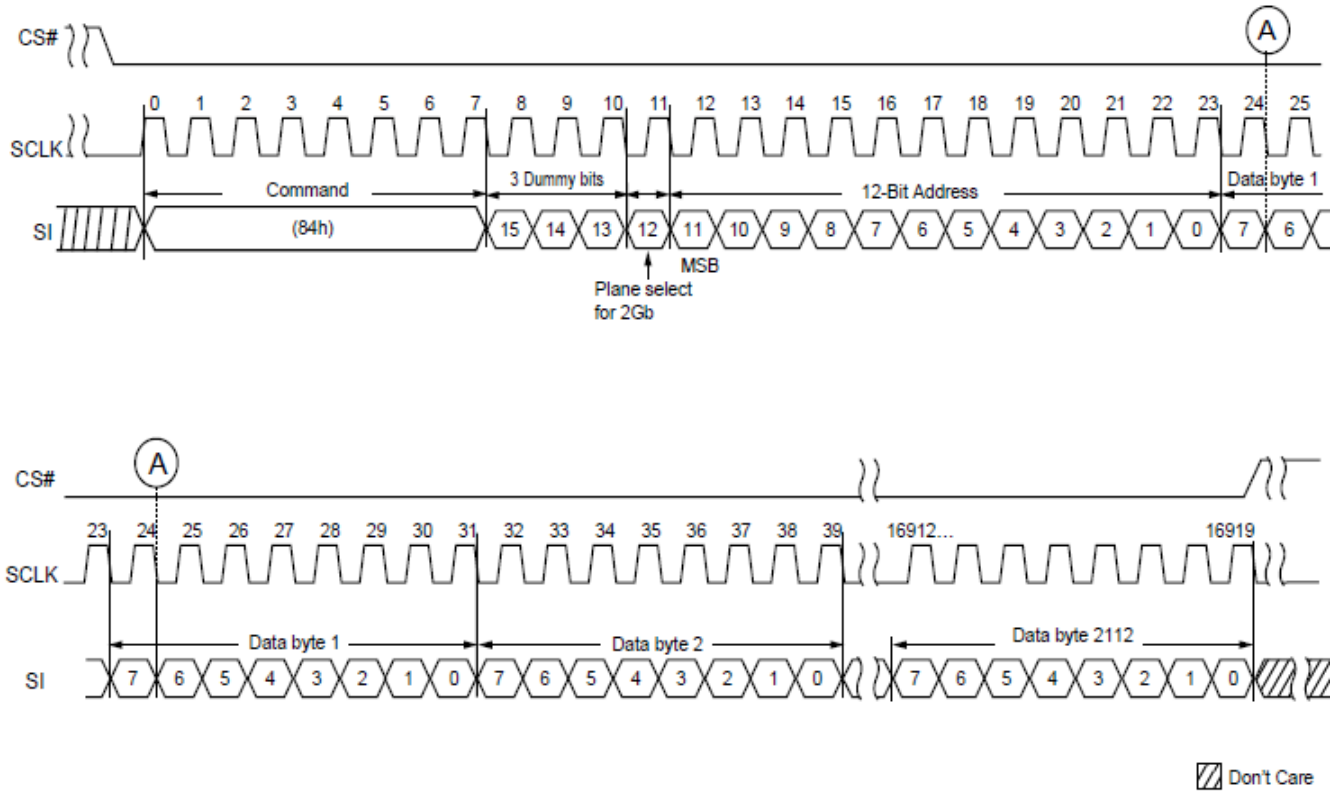


Figure 3.13 Program Load Random Data (84h)

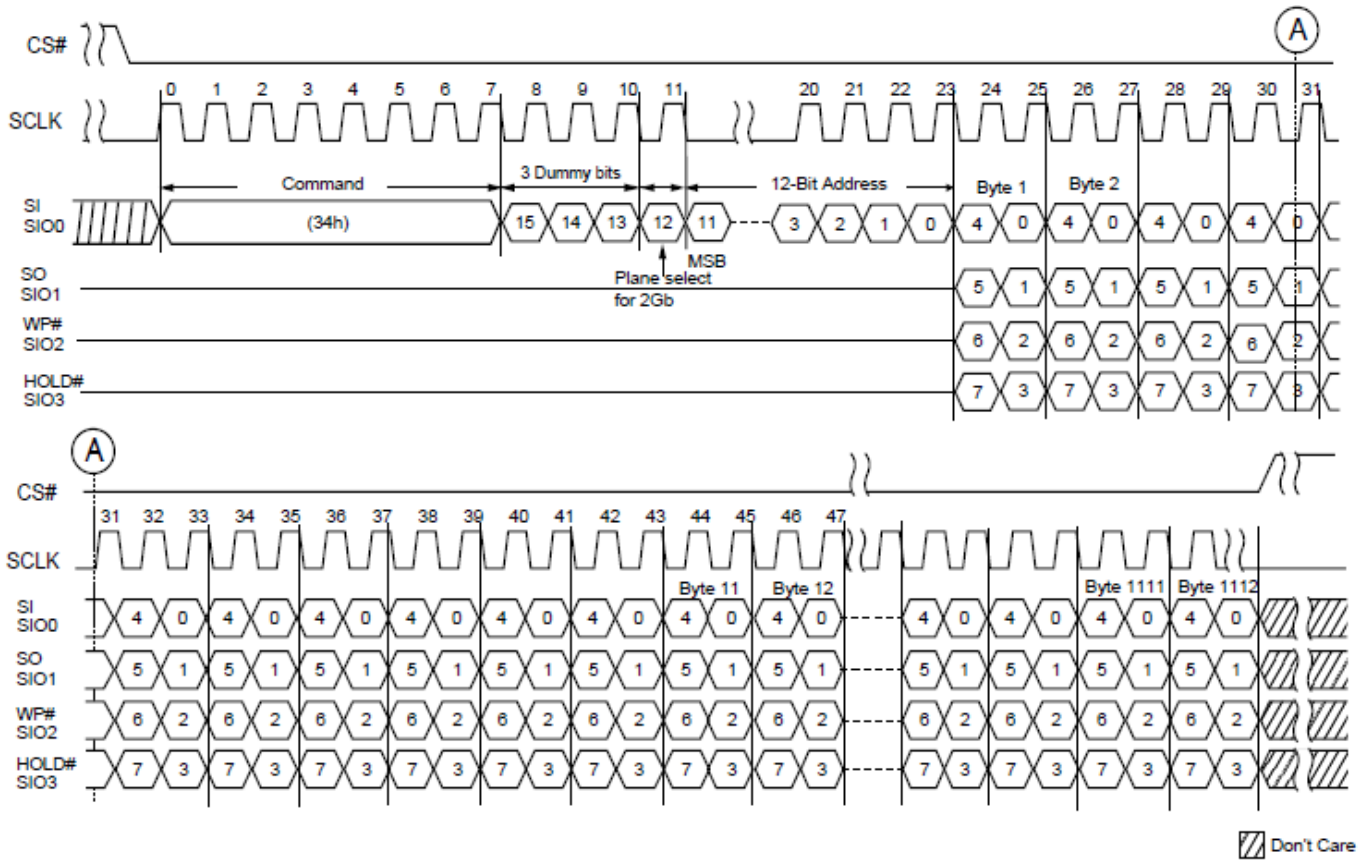


Figure 3.14 Program Load Random Data x4 (34h)

The INTERNAL DATA MOVE command sequence programs or replaces data in a page with existing data. The INTERNAL DATA MOVE command sequence is as follows:

- 13h (PAGE READ to cache)
- 06h (WRITE ENABLE)
- 84h (PROGRAM LOAD RANDOM DATA) or 34h (PROGRAM LOAD RANDOM DATA x4)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

Prior to performing an internal data move operation, the target page content must be read into the cache register. This is done by issuing a PAGE READ (13h) command. The PAGE READ command must be followed with a WRITE ENABLE (06h) command in order to change the contents of memory array. After the WRITE ENABLE command is issued, the PROGRAM LOAD RANDOM DATA (84h or 34h) command can be issued.

This command consists of an 8-bit Op code, followed by 3 dummy bits, a 1-bit plane select address and a 12-bit column address. New data is loaded in the 12-bit column address. If the random data is not sequential, another PROGRAM LOAD RANDOM DATA (84h or 34h) command must be issued with the new column address. After the data is loaded, a PROGRAM EXECUTE (10h) command can be issued to start the programming operation.

See **Figure 3.13, 3.14, 3.12**.

3.8 BLOCK ERASE

The BLOCK ERASE (D8h) command is used to erase at the block level. The blocks are organized as 64 pages per block, 2112 bytes per page (2048 + 64 bytes). Each block is 132 Kbytes. The BLOCK ERASE command (D8h) operates on one block at a time. The command sequence for the BLOCK ERASE operation is as follows:

- 06h (WRITE ENBALE command)
- D8h (BLOCK ERASE command)
- 0Fh (GET FEATURES command to read the status register)

Prior to performing the BLOCK ERASE operation, a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE command must be executed in order to set the WEL bit. If the WRITE ENABLE command is not issued, then the rest of the erase sequence is ignored. A WRITE ENABLE command must be followed by a BLOCK ERASE (D8h) command. This command requires a 24-bit address consisting of 7 dummy bits followed by an 17-bit row address.

After the row address is registered, the control logic automatically controls timing and erase-verify operations. The device is busy for tBERS time during the BLOCK ERASE operation.

The GET FEATURES (0Fh) command can be used to monitor the status of the operation.

See **Figure 19.**

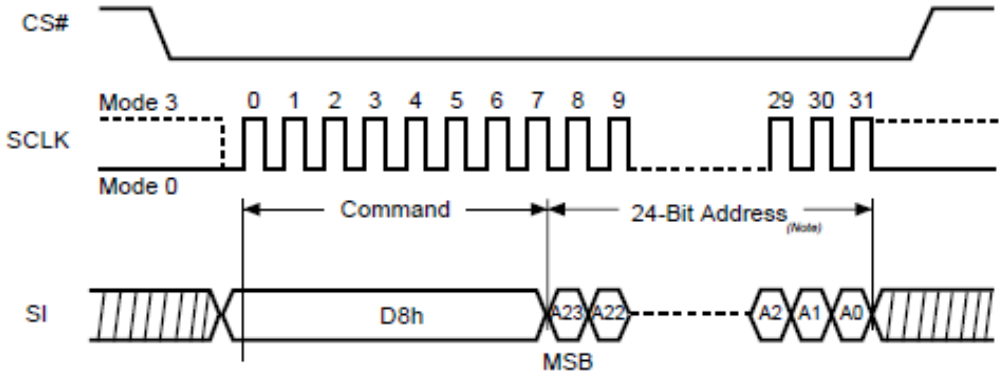


Figure 3.15 Block Erase

3.9 Block Lock Feature.

The block lock feature provides the ability to protect the entire device, or ranges of blocks, from the PROGRAM and ERASE operations. After power-up, the device is in the “locked” state, i.e., bits 1, 2, 3, 4, and 5 of the block lock register are set to 1. To unlock all the blocks, or a range of blocks, the SET FEATURES command must be issued with the A0h feature address, including the data bits shown in Table 7. When BRWD is set and WP is LOW, none of the writable bits (1, 2, 3, 4, 5, and 7) in the block lock register can be set.
When an ERASE command is issued to a locked block, the erase failure, 04h, is returned. When a PROGRAM command is issued to a locked block, program failure, 08h, is returned.

BP2	BP1	BP0	Invert	Complementary	Protection
0	0	0	x	x	all unlocked
0	0	1	0	0	upper 1/64 locked
0	1	0	0	0	upper 1/32 locked
0	1	1	0	0	upper 1/16 locked
1	0	0	0	0	upper 1/8 locked
1	0	1	0	0	upper 1/4 locked
1	1	0	0	0	upper 1/2 locked
1	1	1	x	x	all locked (default)
0	0	1	1	0	lower 1/64 locked
0	1	0	1	0	lower 1/32 locked
0	1	1	1	0	lower 1/16 locked
1	0	0	1	0	lower 1/8 locked
1	0	1	1	0	lower 1/4 locked
1	1	0	1	0	lower 1/2 locked
0	0	1	0	1	lower 63/64 locked
0	1	0	0	1	lower 31/32 locked
0	1	1	0	1	lower 15/16 locked
1	0	0	0	1	lower 7/8 locked
1	0	1	0	1	lower 3/4 locked
1	1	0	0	1	Block0
0	0	1	1	1	upper 63/64 locked
0	1	0	1	1	upper 31/32 locked
0	1	1	1	1	upper 15/16 locked
1	0	0	1	1	upper 7/8 locked
1	0	1	1	1	upper 3/4 locked
1	1	0	1	1	Block0

Table 3.4 Definition of Protectiong Bits

3.10 OTP Feature.

The serial device offers a protected, one-time programmable NAND Flash memory area. 30 full pages (2112 bytes per page) are available on the device, and the entire range is guaranteed to be good. Customers can use the OTP area any way they want; typical uses include programming serial numbers, or other data, for permanent storage.
To access the OTP feature, the user must issue the SET FEATURES command, followed by feature address B0h. When the OTP is ready for access, pages 02h–1Fh can be programmed in sequential order. The PROGRAM LOAD (02h) and PROGRAM EXECUTE (10h) commands can be used to program the pages. Also, the PAGE READ (13h) command can be used to read the OTP area. The data bits used in feature address B0h to enable OTP access are shown in the table below.

To access OTP, perform the following command sequence:

- Issue the SET FEATURES register write (1Fh)
- Issue the OTP feature address (B0h)
- Issue the PAGE PROGRAM or PAGE READ command

It is important to note that after bits 6 and 7 of the OTP register are set by the user, the OTP area becomes read-only and no further programming is supported. For OTP states, see the following table.

OTP Protection Bit	OTP Enabled Bit	State
0	0	Normal operation
0	1	Access the Secure OTP
1	0	Not applicable
1	1	OTP Protection by using the Program Execution command (10h)

Table 3.5 OTP States

3.11 Status Register

The NAND Flash device has an 8-bit status register that software can read during the device operation. The status register will output the status of the operation. The description of data bits from status register are shown in the following table.

SR Bit	Bit Name	Description
SR[0] (OIP)	Operation in progress	The bit value indicates whether the device is busy in operations of read/program execute/ erase/ reset command. 1: Busy, 0: Ready
SR[1] (WEL)	Write enable latch	The bit value indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, and then the device can accept program/ erase command. 1: write enable, 0: not write enable The bit value will be cleared (as "0") by issuing Write Disable command(04h).
SR[2] (ERS_Fail)	Erase fail	The bit value shows the status of erase failure or if host erase any invalid address or protected area (including protected blocks or protected Secure OTP area). 0: Passed, 1: Failed The bit value will be cleared (as "0") by RESET command or at the beginning of the block erase command operation.
SR[3] (PGM_Fail)	Program fail	The bit value shows the status of program failure or if host program any invalid address or protected area (including protected blocks or protected Secure OTP area). 0: Passed, 1: Failed The bit value will be cleared (as "0") by RESET command or during the program execute command operation.
SR[5:4] (ECC_S1, ECC_S0)	ECC Status	The bit shows the status of ECC as below: 00b = 0 bit error 01b = 1 ~ 4 bits error and been corrected. 10b = More than 4-bit error and not corrected. 11b = Reserved The value of ECC_Sx (S1:S0) bits will be clear as "00b" by Reset command or at the start of the Read operation. After a valid Read operation completion, the bit will be updated to reflect the ECC status of the current valid Read operation. The ECC_Sx (S1:S0) value reflects the ECC status of the content of the page 0 of block 0 after a power-on reset. If the internal ECC is disabled by the Set feature command, the ECC_ Sx(S1:S0) are invalid.
SR[6:7]	Reserved	

Table 3.6 Status Register Bit Descriptions

3.12 ECC Protection

The serial device offers data corruption protection by offering 4-bit internal ECC.
READs and PROGRAMs with internal ECC can be enabled or disabled by setting the ECC bit in the OTP register.
ECC is enabled after device power up, so the default READ and PROGRAM commands operate with internal ECC in the "active" state.
To enable/disable ECC, perform the following command sequence:

- Issue the SET FEATURES register write (1Fh).
- Issue the OTP feature address (B0h).
- Then:
  – To enable ECC Set Bit 4, ECC Enable, to 1.
  – To disable ECC Clear Bit 4, ECC Enable, to 0.

During a PROGRAM operation, the device calculates an ECC code on the 2k page in the cache register, before the page is written to the NAND Flash array. The ECC code is stored in the spare area of the page.
During a READ operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the ECC code value read from the array. If a 1- to 4-bit error is detected, the error is corrected in the cache register. Only corrected data is output on the I/O bus. The ECC status bit indicates if the error correction was successful. The ECC Protection table below shows the ECC protection scheme used throughout a page.

With internal ECC, the user must accommodate the following:

- The ECC protection coverage: please refer to Table 10. The Distribution of ECC Segment and Spare Area. Only the grey areas are under internal ECC protection when the internal ECC is enabled.
- The number of partial-page program is not 4 in an ECC segment, the user need to program the main area (512B)+Metadata1(4B) at one program time, so the ECC parity code can be calculated properly and stored in the additional hidden spare area.

Area	Main Area (0)	Main Area (1)	Main Area (2)	Main Area (3)	Spare(0)				Spare(1)			
					M2		M1	R2	M2		M1	R2
Addr. (Start)	000h	200h	400h	600h	800h	802h	804h	808h	810h	812h	814h	818h
Addr. (End)	1FFh	3FFh	5FFh	7FFh	801h	803h	807h	80Fh	811h	813h	817h	81Fh
Size	512(B)	512(B)	512(B)	512(B)	2(B)	2(B)	4(B)	8(B)	2(B)	2(B)	4(B)	8(B)

Area	Main Area (0)	Main Area (1)	Main Area (2)	Main Area (3)	Spare(2)				Spare(3)			
					M2		M1	R2	M2		M1	R2
Addr. (Start)	000h	200h	400h	600h	820h	822h	824h	828h	830h	832h	834h	838h
Addr. (End)	1FFh	3FFh	5FFh	7FFh	821h	823h	827h	82Fh	831h	833h	837h	83Fh
Size	512(B)	512(B)	512(B)	512(B)	2(B)	2(B)	4(B)	8(B)	2(B)	2(B)	4(B)	8(B)

Table 3.7 The Distribution of ECC Segment and Spare Area

R1/R2: Reserved
M2: Metadata 2
M1: Metadata 1
Grey area: Under ECC protection

4 Device Parameters

Parameter	Symbol	Min	Typ	Max	Unit
Valid Block Number	N_{VB}	2008		2048	Blocks

Table 4.1 Valid Blocks Number

The First block (Block 0) is guaranteed to be a valid block at the time of shipment.
The specification for the minimum number of valid blocks is applicable over lifetime.

Symbol	Parameter	Value		Unit
		1.8V	3.3V	
T_A	Ambient Operating Temperature	0 to 70	0 to 70	°C
	Ambient Operating Temperature	–40 to 85	–40 to 85	°C
	Ambient Operating Temperature	–40 to 105	–40 to 105	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	–65 to 150	°C
V_{IO}	Input or Output Voltage	–0.6 to 2.7	–0.6 to 4.6	V
V_{CC}	Supply Voltage	–0.6 to 2.7	–0.6 to 4.6	V

Table 4.2 Absolute Maximum Ratings

.

Parameter		Symbol	Test Conditions	1.8Volt			3.3Volt			Unit
				Min	Typ	Max	Min	Typ	Max	
Operating Current	Sequential Read	I_{CC1}	104Mhz, CS#=V_{IL}, I_{OUT}=0mA	-	10	20	-	15	30	mA
	Program	I_{CC2}	-	-	10	20	-	15	30	mA
	Erase	I_{CC3}	-	-	10	20	-	15	30	mA
Stand-by Current (TTL)		I_{CC4}	CS#= V_{CC}, VIN=VCC or GND	-	-	1			1	mA
Stand-By Current (CMOS)		I_{CC5}	CS#=V_{CC}, VIN=VCC or GND	-	10	50		10	50	uA
Input Leakage Current		I_{LI}	V_{IN}=0 to Vcc (max)	-	-	±10		-	±10	uA
Output Leakage Current		I_{LO}	V_{OUT}=0 to Vcc(max)	-	-	±10		-	±10	uA
Input High Voltage		V_{IH}	-	0.8xV_{CC}	-	V_{CC} +0.3	0.8x V_{CC}	-	V_{CC} +0.3	V
Input Low Voltage		V_{IL}	-	-0.3	-	0.2x V_{CC}	-0.3	-	0.2xV_{CC}	V
Output High Voltage Level		V_{OH}	I_{OH} = -100uA	V_{CC}-0.1	-	-				V
			I_{OH} = -400uA				2.4	-	-	V
Output Low Voltage Level		V_{OL}	I_{OL} = 100uA	-	-	0.1				V
			I_{OL} = 2.1mA				-	-	0.4	V

Table 4.3 DC and Operating Characteristics

Parameter	Value	
	1.8Volt	3.3Volt
Input Pulse Levels	0V to V_{CC}	0V to V_{CC}
Input Rise and Fall Times	5ns	5ns
Input and Output Timing Levels	V_{CC} / 2	V_{CC} / 2
Output Load (1.7V – 1.95V & 2.5V - 3.6V)	1 TTL GATE and CL=30pF	1 TTL GATE and CL=30pF

Table 4.4 AC Test Conditions

Item	Symbol	Test Condition	Min	Max	Unit
Input / Output Capacitance (1)	$C_{I/O}$	V_{IL} = 0V	-	10	pF
Input Capacitance (1)	C_{IN}	V_{IN} = 0V	-	10	pF

Table 4.5 Ping Capacitance (TA=25C,f=1.0MHz)

Parameter		Symbol	Min		Typ		Max		Unit
			1.8Volt	3.3Volt	1.8Volt	3.3Volt	1.8Volt	3.3Volt	
Read Time		t_R	-	-	-	-	25	25	us
Read Time with internal ECC enabled		t_{R_ECC}	70	60	-	-	100	90	us
Program Time		t_{PROG}	-	-	300	300	700	700	us
Program Time with internal ECC enabled		t_{PROG_ECC}	-	-	320	320	700	700	us
Number of partial Program Cycles in the same page	Main + Spare Array	NOP	-	-	-	-	4	4	Cycle
Block Erase Time		t_{BERS}	-	-	2.0	2.0	10	10	ms

Table 4.6 Read/Program/Erase Characteristics

Parameter	Symbol	1.8/3.3 Volt		Unit
		Min	Max	
Clock Frequency	f_C		104	MHz
Clock HIGH time	t_{WH}	4		ns
Clock LOW time	t_{WL}	4		ns
Command deselect time	t_{CS}	100		ns
Chip select# hold time	t_{CHSH}	5		ns
Chip select# setup time	t_{SLCH}	5		ns
Chip select# non-active setup time	t_{SHCH}	5		ns
Chip select# non-active hold time	t_{CHSL}	5		ns
Output disable time	t_{DIS}		20	ns
Hold# non-active setup time relative to SCLK	t_{HC}	5		ns
Hold# setup time relative to SCLK	t_{HD}	5		ns
Data input hold time	t_{HDDAT}	3.5		ns
Output hold time	t_{HO}	1		ns
Hold to output High-Z	t_{HZ}		15	ns
Hold to output low-Z	t_{LZ}		15	ns
Data input setup time	t_{SUDAT}	3.5		ns
Clock LOW to output Valid	t_V		8	ns
WP# hold time	t_{WPH}	100		ns
WP# setup time	t_{WPS}	20		ns
HOLD# high hold time relative to SCLK	t_{CHHH}	5		ns
HOLD# low hold time relative to SCLK	t_{CHHL}	5		ns
Device Resetting Time (Read/Program/Erase)	t_{RST}		5/10/500 (1)	us

Table 4.7 AC Timing Characteristics

NOTE:

(1) If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us

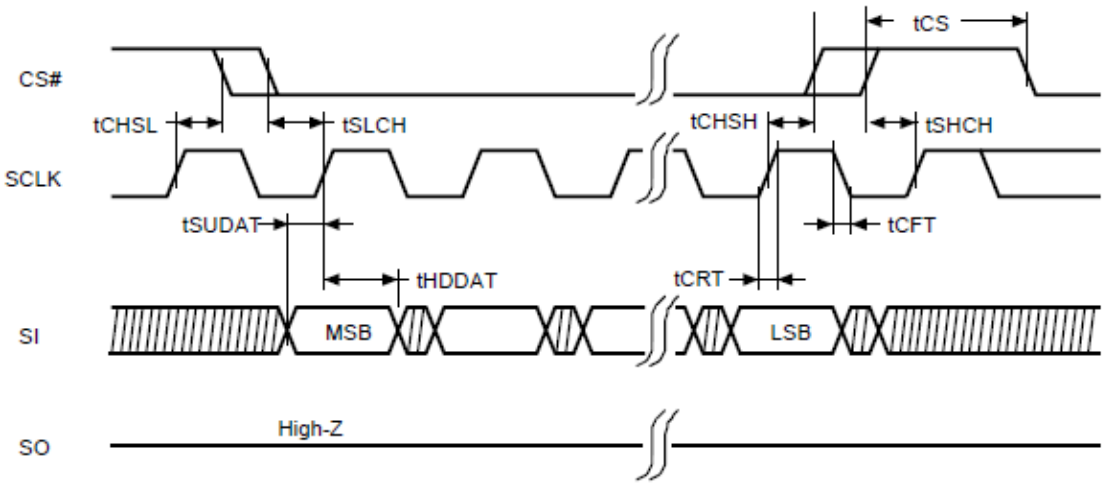


Figure 4.1 Serial Input Timing

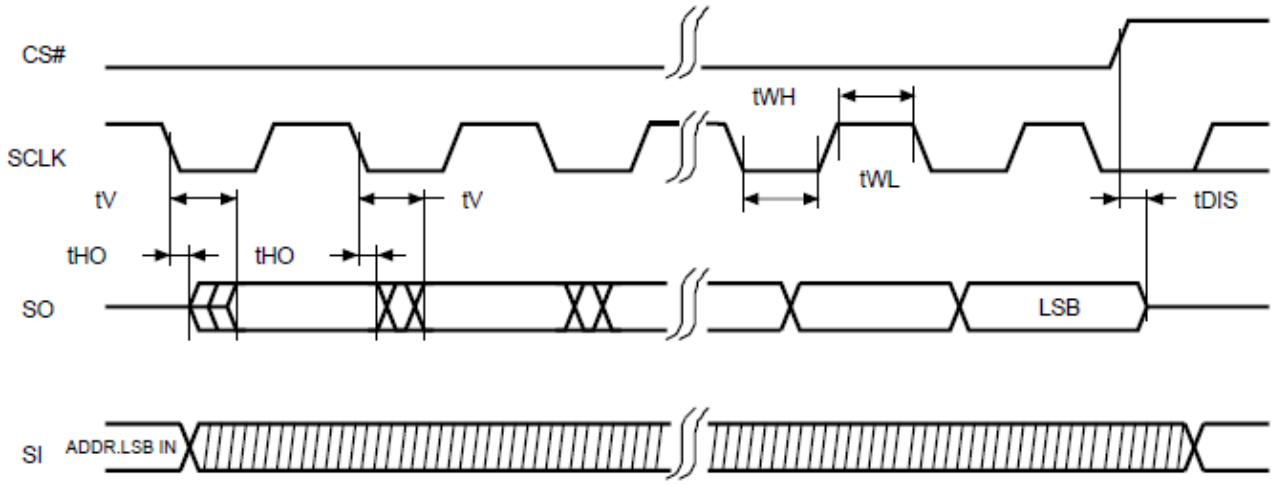


Figure 4.2 Serial Output Timing

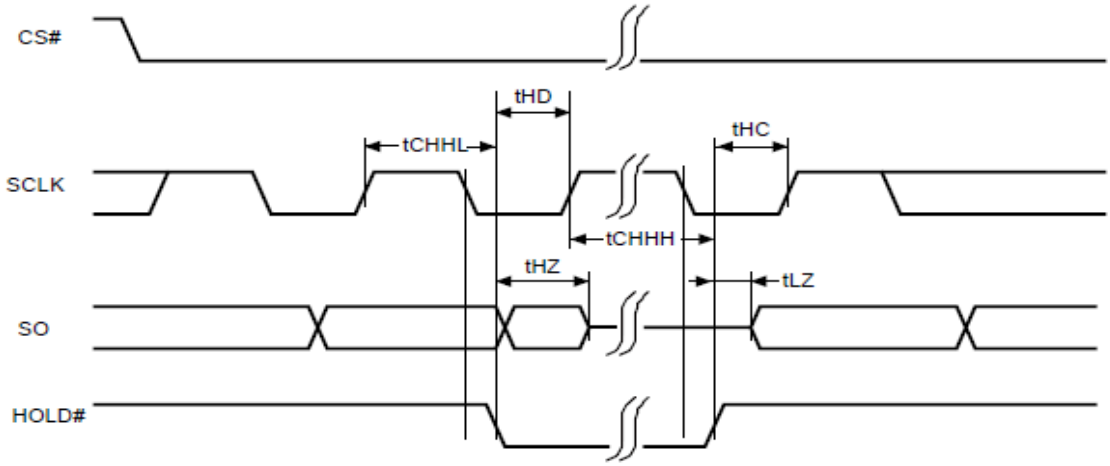


Figure 4.3 Hold Timing

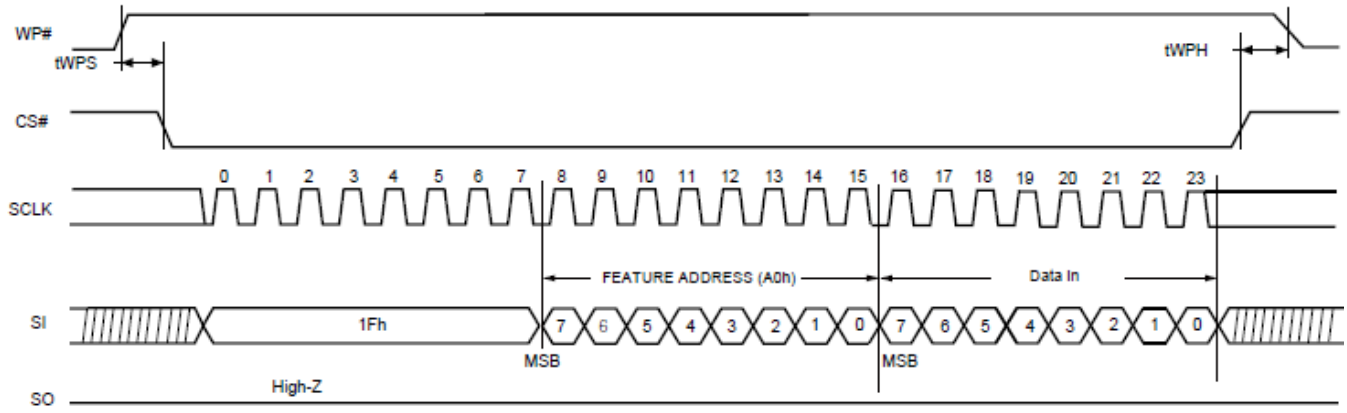


Figure 4.4 WP# Setup/Hold Timing When BPRWD=1

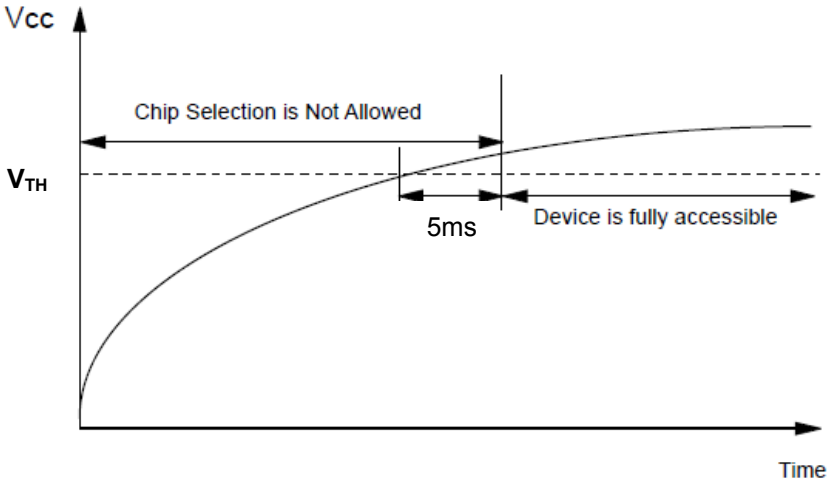


Figure 4.5 Power on Sequence

Note : V_{TH} = **1.5** Volt for 1.8 Volt Supply devices; **2.5** Volt for 3.3 Volt Supply devices

5 Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased (FFh). The Bad Block Information is written prior to shipping. Any block where the 1st Byte in the spare area of the 1st or 2nd page (if the 1st page is Bad) does not contain FFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart

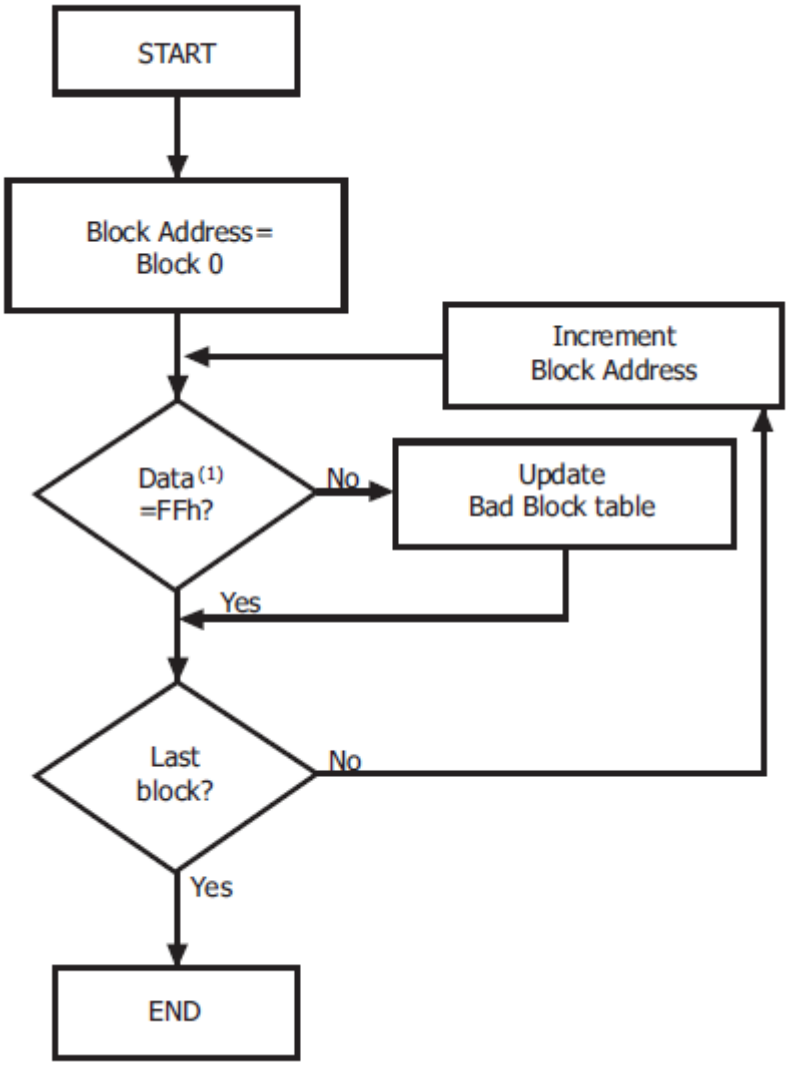


Figure 5.1 Bad Block Management Flowchart

Over the lifetime of the device additional Bad Blocks may develop. In this case the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.
The failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block.

Failure Mode		Sequence
Write	Erase Failure	Block Replacement
	Program Failure	Block Replacement
Read	Read Failure	ECC

Table 5.1 Block Failure

Block Replacement flow is as below
1.When an error happens in the nth page of the Block 'A' during erase or program operation.
2.Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
3.Copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
4.Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

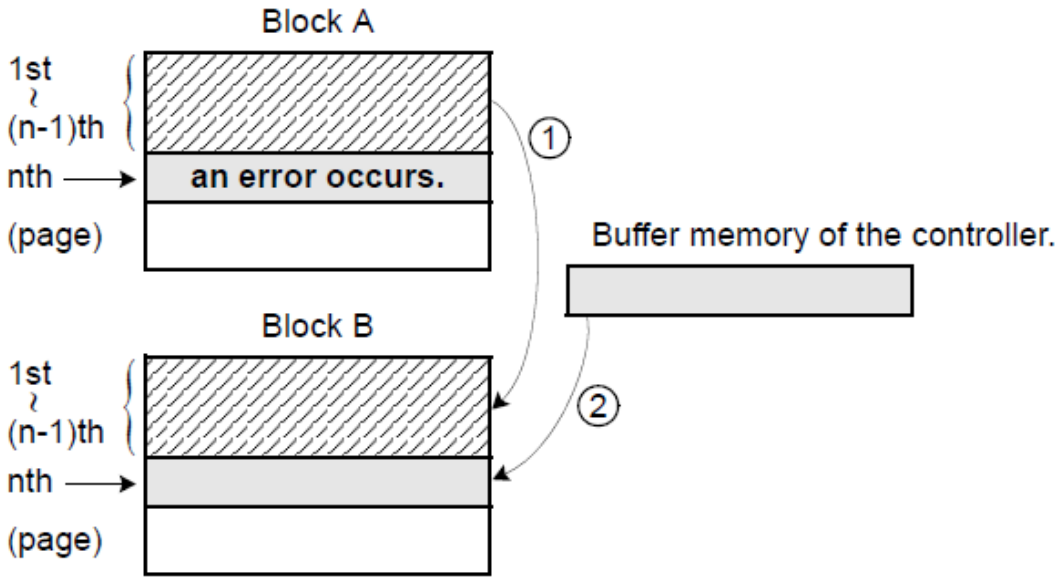


Figure 5.2 Bad Block Replacement

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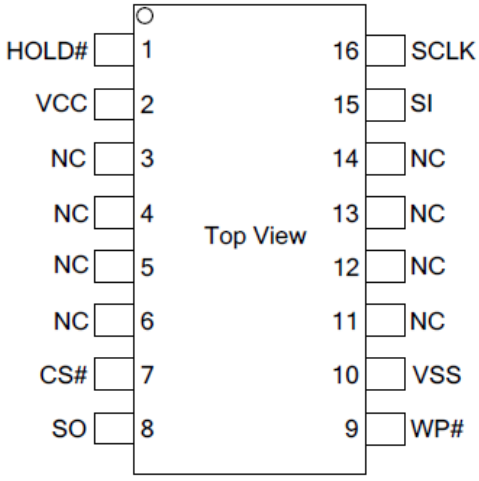
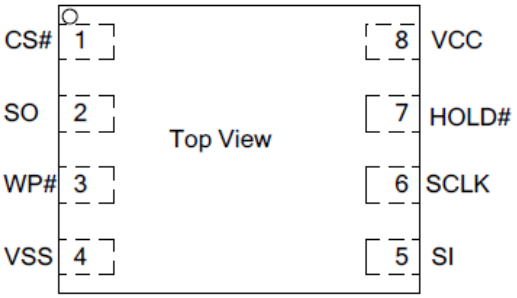
6 Supported Packages

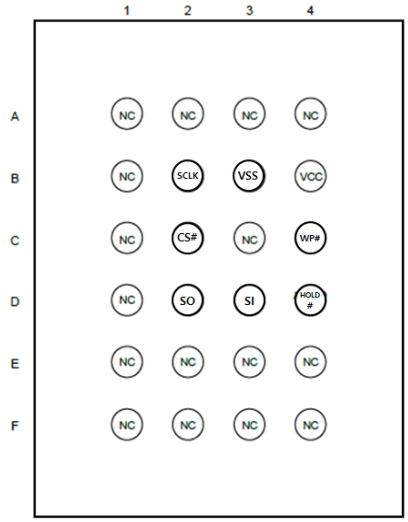
6.1 Pin configuration



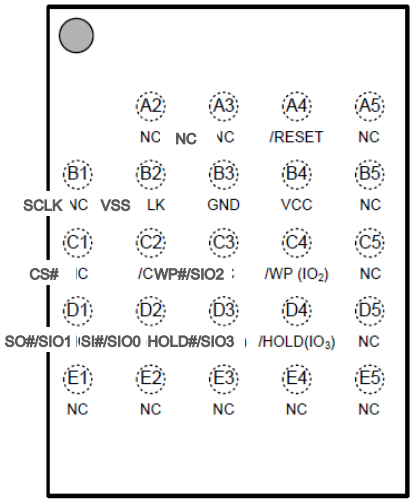
16-LEAD SOP



8-LEAD WSON



BGA24(6x4 Ball Array)

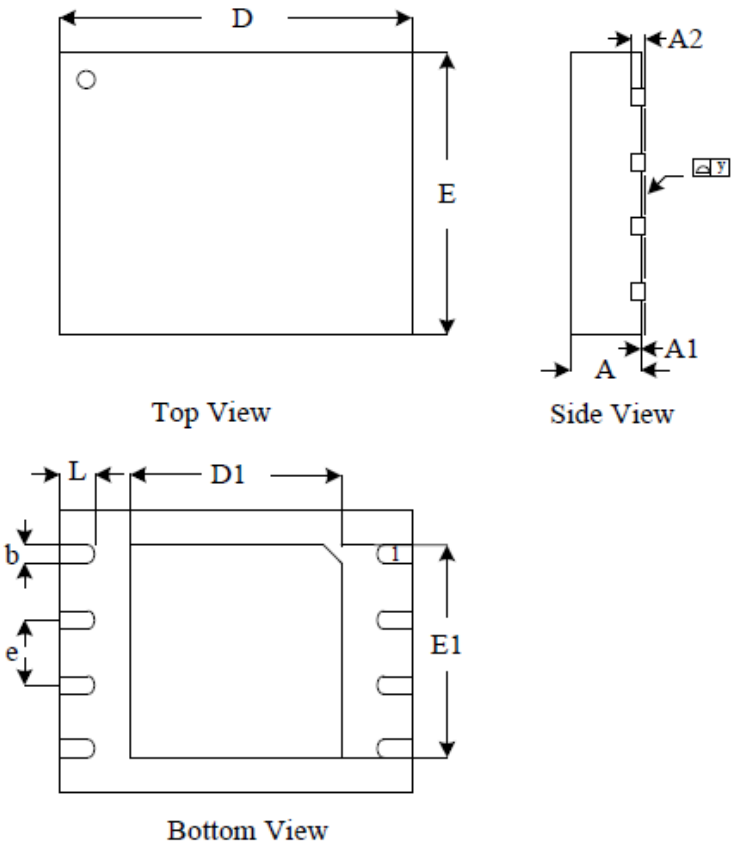


BGA24(5x5 Ball Array)

Figure 6.1 Pin Configuration

6.2 Package dimension

WSON(8*6mm)

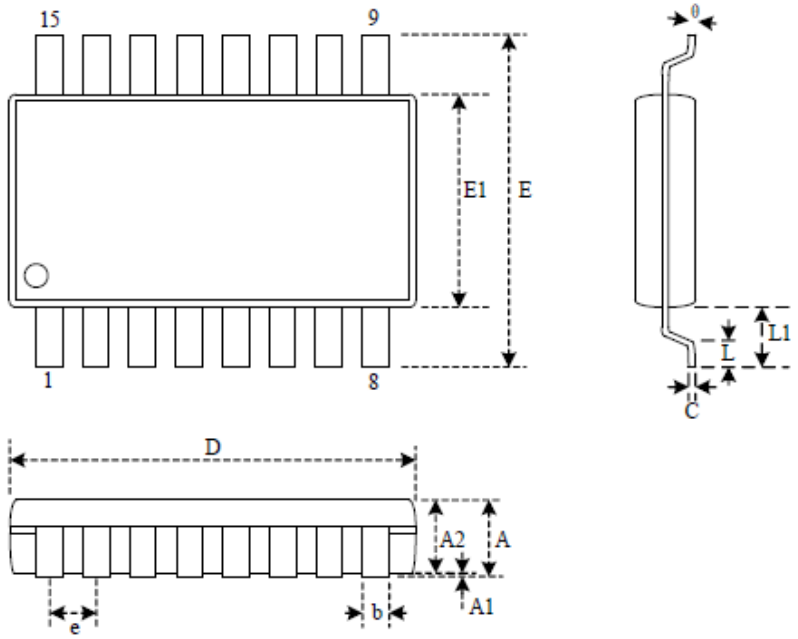


Dimensions

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e	y	L
mm	Min	0.70			0.35	7.95	3.25	5.95	4.15		0.00	0.40
	Nom	0.75		0.20	0.40	8.00	3.40	6.00	4.30	1.27		0.50
	Max	0.80	0.05		0.45	8.05	3.50	6.05	4.40		0.05	0.60
Inch	Min	0.028			0.014	0.313	0.128	0.234	0.163		0.00	0.016
	Nom	0.030		0.008	0.016	0.315	0.134	0.236	0.169	0.05		0.020
	Max	0.032	0.002		0.019	0.317	0.138	0.238	0.173		0.002	0.024

Figure 6.2 WSON (8*6mm)

SOP16

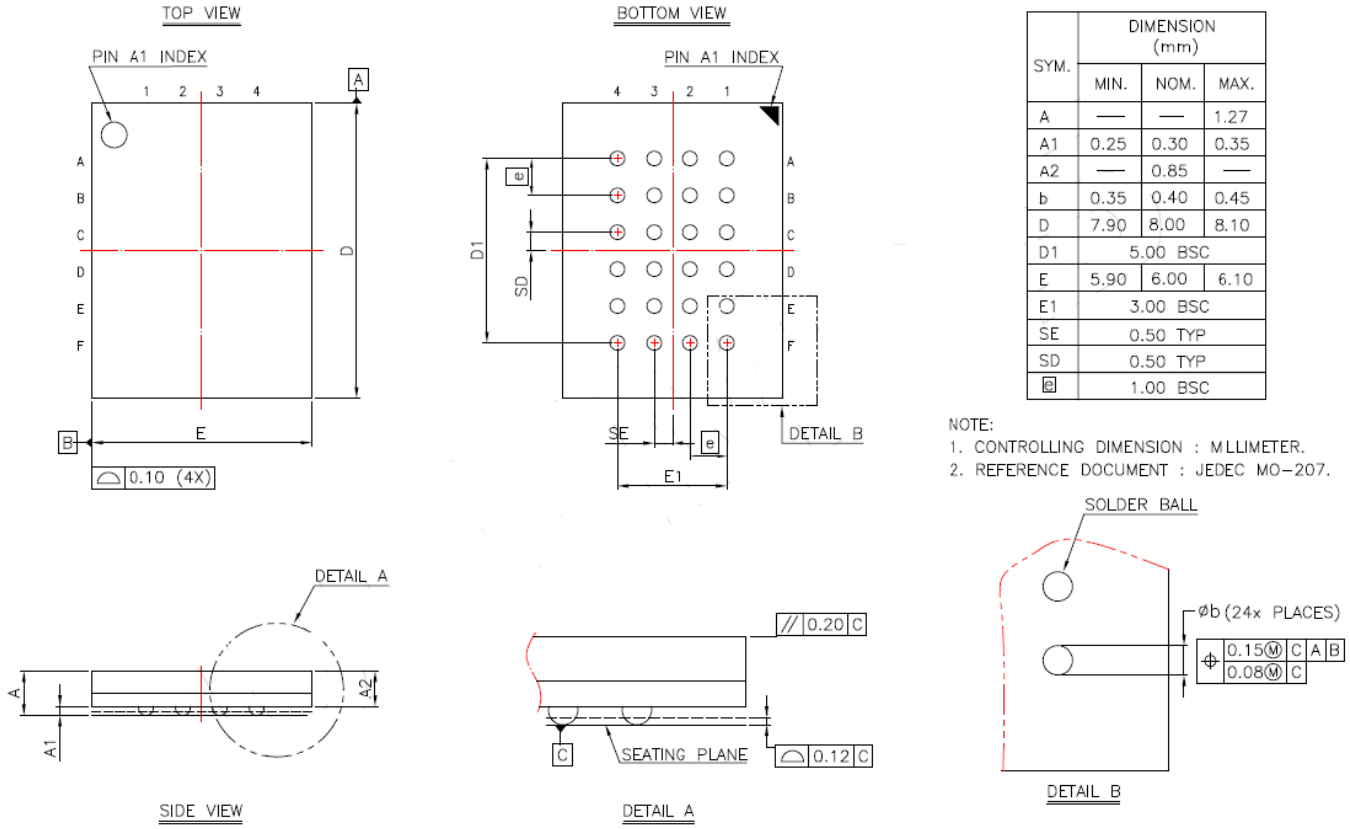


Dimensions

Symbol / Unit		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min	2.36	0.10	2.24	0.36	0.20	10.10	10.10	7.42		0.40	1.31	0.51	0
	Nom	2.55	0.20	2.34	0.41	0.25	10.30	10.35	7.52	1.27	0.84	1.44	0.64	5
	Max	2.75	0.30	2.44	0.51	0.30	10.50	10.60	7.60		1.27	1.57	0.77	8
Inch	Min	0.093	0.004	0.088	0.014	0.008	0.397	0.397	0.292		0.016	0.052	0.020	0
	Nom	0.100	0.008	0.092	0.016	0.010	0.405	0.407	0.296	0.050	0.033	0.057	0.025	5
	Max	0.108	0.012	0.096	0.020	0.012	0.413	0.417	0.299		0.050	0.062	0.030	8

Figure 6.3 SOP16

BGA24(6x4 Ball Array)

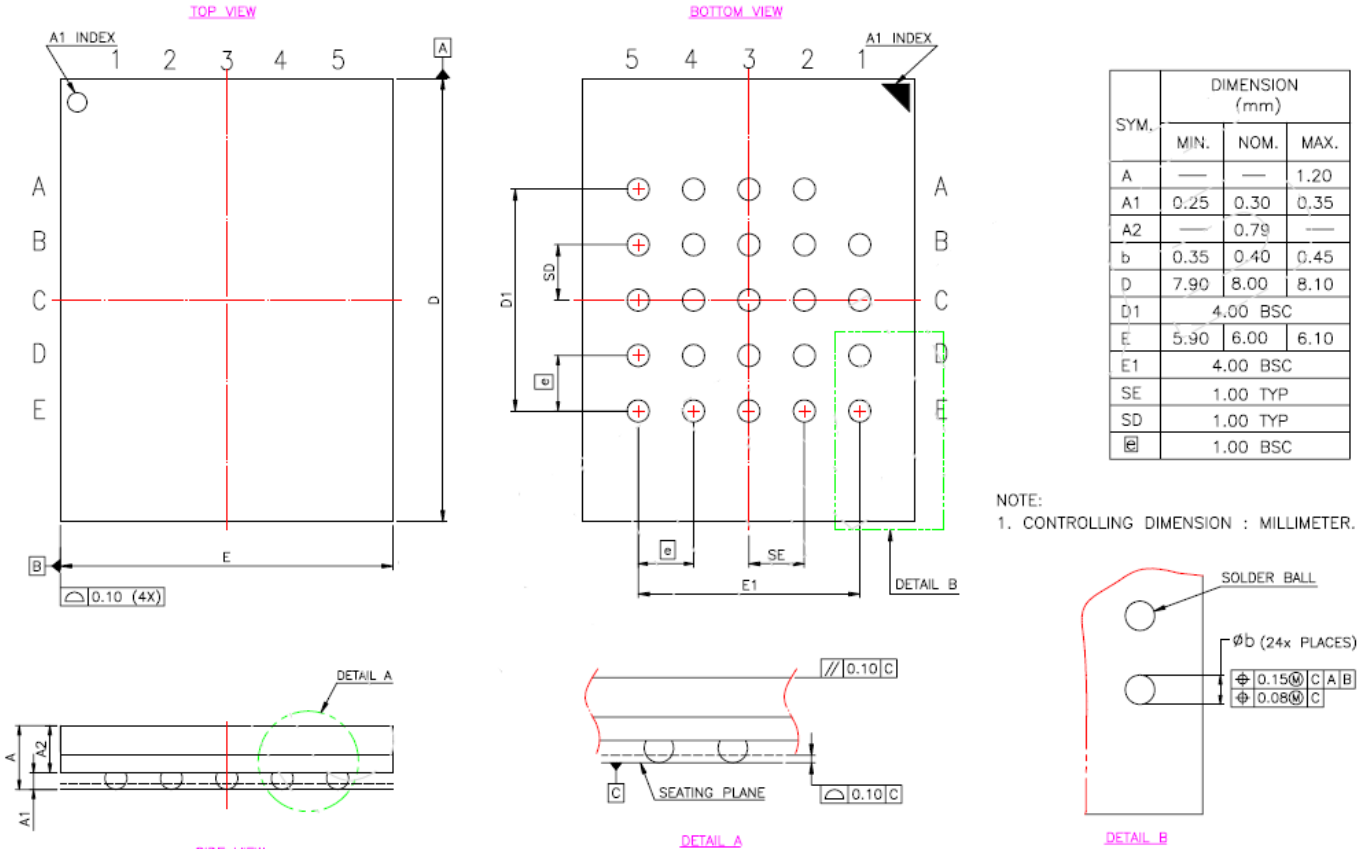


SYM.	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	—	—	1.27
A1	0.25	0.30	0.35
A2	—	0.85	—
b	0.35	0.40	0.45
D	7.90	8.00	8.10
D1	5.00 BSC		
E	5.90	6.00	6.10
E1	3.00 BSC		
SE	0.50 TYP		
SD	0.50 TYP		
e	1.00 BSC		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.

Figure 6.4 BGA24(6x4 Ball Array)

BGA24(5x5 Ball Array)



SYM.	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.25	0.30	0.35
A2	—	0.79	—
b	0.35	0.40	0.45
D	7.90	8.00	8.10
D1	4.00 BSC		
E	5.90	6.00	6.10
E1	4.00 BSC		
SE	1.00 TYP		
SD	1.00 TYP		
e	1.00 BSC		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.

Figure 6.5 BGA24(5x5 Ball Array)